能源革命的驱动力-碳化硅引领未来

宽禁带半导体-安森美碳化硅方案

2024-04-09

熊壮

WPI-PMO华南技术支援组

Agenda

- 半导体发展历程；
- 宽禁带半导体概述；
- SiC MOSFET应用设计经验分享；
  - SiC MOSFET针对不同拓扑和开关模式的关键参数；
  - SiC MOSFET分立器件并联时均流风险与解决方案；
  - 平面栅工艺SiC MOSFET驱动做0V关断电压可行性；

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半导体材料发展历程

第一代/第二代/第三代半导体材料及主要应用

参考资料：

https://www.onsemi.com/download/application-notes/pdf/and90103-d.pdf

DOI：10.19772/j.cnki.2096-4455.2019.4.028

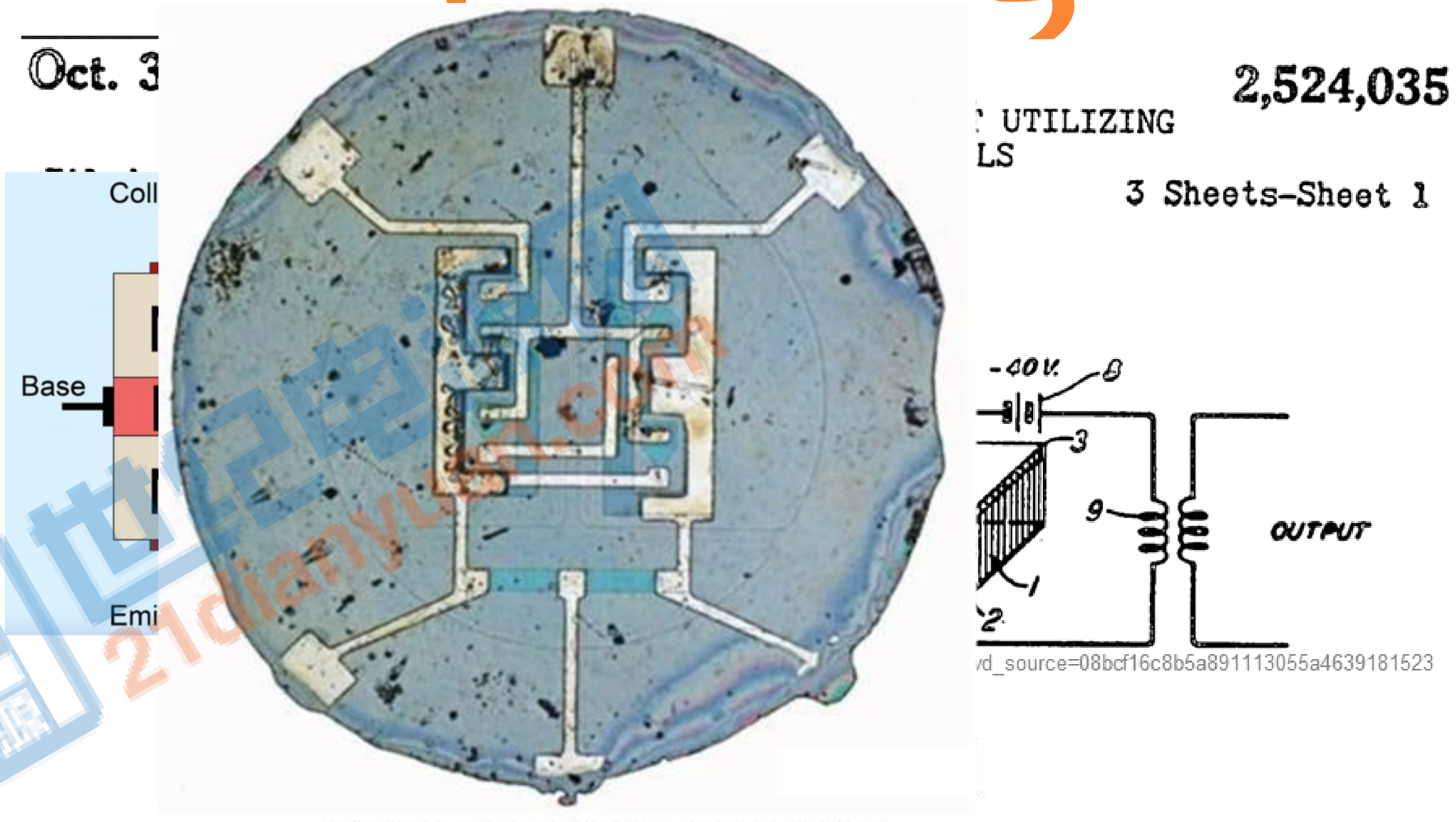
DOI：10.13334/j.0258-8013.pcsee.191728

DOI：11.11985/2016.01.001

半导体材料发展历程概述

第一代、第二代、第三代

- 1906 电子管（真空三极管）
- 1947 锗晶体管(点接触式)
- 1950 BJT锗晶体管（NPN）
- 1954 BJT硅晶体管
- 1959 平面式集成电路 FAIRCHILD
- 1959 MOSFET
- 1980s IGBT



https://zhuanlan.zhihu.com/p/465126898

第一代半导体

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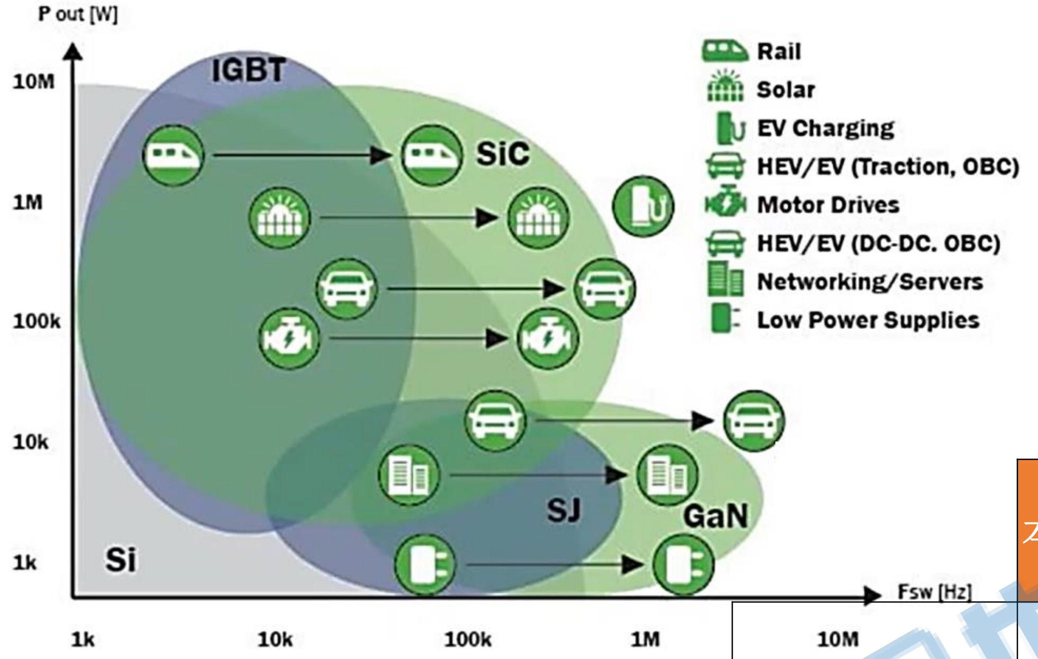
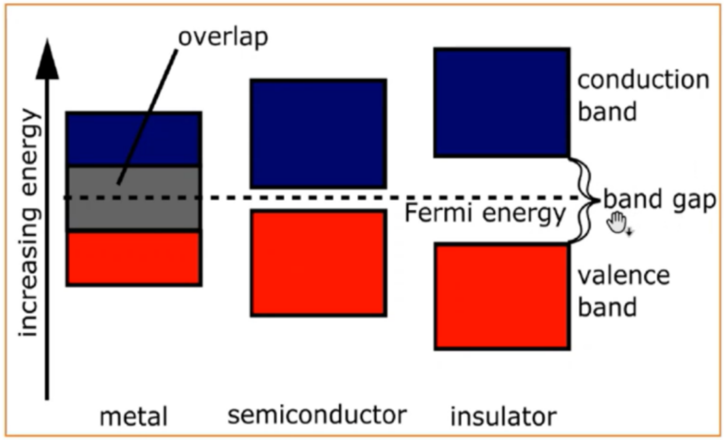
半导体材料优缺点及主要应用



Commercially Available Devices

Device Technology	Working Voltage (V)
Silicon Super-Junction MOSFET	600 – 800V
Silicon IGBT	650 – 6500V
SiC MOSFET	650 – 1700V
GaN HEMT	< 650V



"A comparison of the band gaps of metals, insulators and semiconductors." by inductiveload CC A-SA 2.5

宽禁带：Eg＞2.3 eV

	本征半导体材料	优点	缺点	主要应用
第一代（元素半导体）	硅(Si) 锗(Ge)	技术成熟； 价格便宜；	相对低的热导率； 相对低的温度范围； 相对低的电压范围；	取代了笨重的电子管，硅基半导体材料开创了MOSFET和IGBT为代表的固态电子时代；
第二代（化合物半导体）	砷化镓（GaAs） 磷化铟（InP）	高频特性； 高电流密度； 低噪声；	制造成本高； 热稳定性差；	射频、微波和光电器件； 高灵敏度传感器；
第三代（宽禁带半导体）	碳化硅（SiC） 氮化镓（GaN）	更低的导通电阻； 更高的击穿电压； 更低的结-壳热阻； 更低的开关损耗；	制造难度大； 良率低；	储能、光伏、充电桩 汽车OBC/Traction/E-compressor 电池化成、特种电源（电镀/电焊） …

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宽禁带半导体概述

参考资料：

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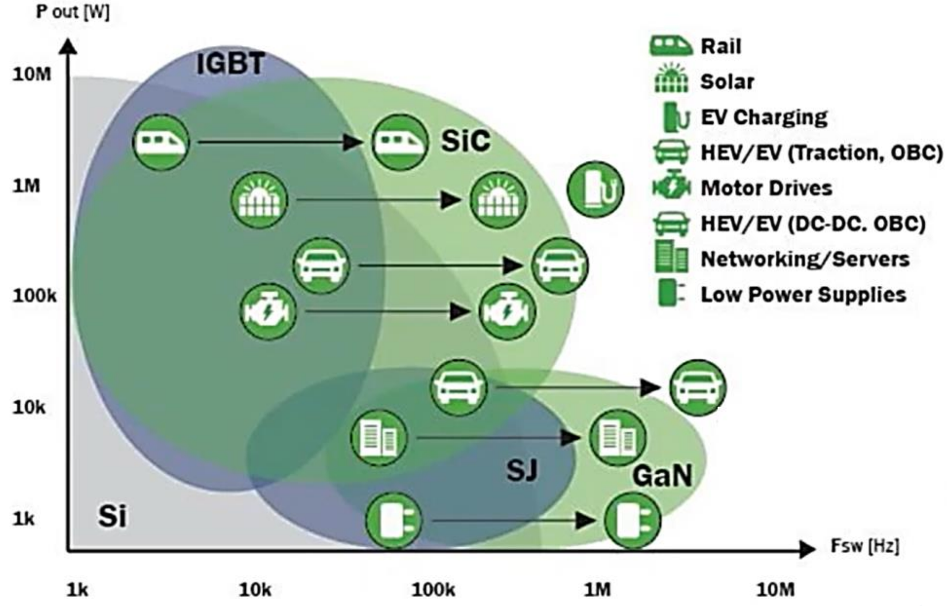
宽禁带半导体与硅参数对比



SiC VS. Si

- 千分之一的比导通电阻；
- 十倍的击穿场强；
- 四倍的导热率；
- 三倍的禁带宽度；

属性	硅	4H-SiC	GaN
带隙能量 (eV)	1.12	3.26	3.5
电子迁移率 (cm^2/Vs)	1400	900	1250
空穴迁移率 (cm^2/Vs)	600	100	200
击穿场 (MV/cm)	0.3	3	3
热导率 (W/cm°C)	1.5	4.9	1.3
最高结温 (°C)	150	600	400

- 更宽的带隙能量意味着能够承受更高的击穿电压
- 相同数量级的迁移率意味着适合高频开关应用场景
- 更高的击穿场意味着更小器件厚度和导通电阻
- 更高的热导率意味着更低温升
- 更高的结温意味着更适合高温大电流应用场景

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碳化硅器件较硅基器件优势

更低的损耗→更高的效率

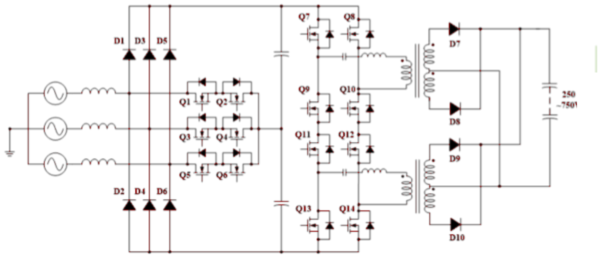
系统级
- 小型化
- 轻质化
- 成本效益

简化拓扑
:更低的Rds(on)
和更高的耐压

600 / 650V SJ MOSFET

3Φ Vienna PFC (~50kHz)

Series FB LLC (100~250kHz)



SiC MOSFET
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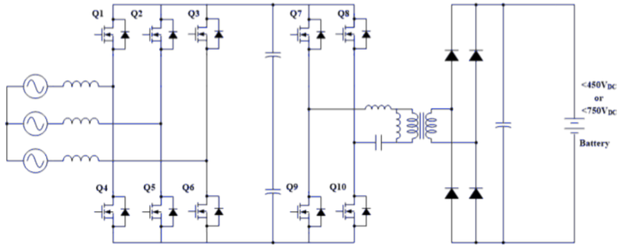
1200V SiC MOSFET

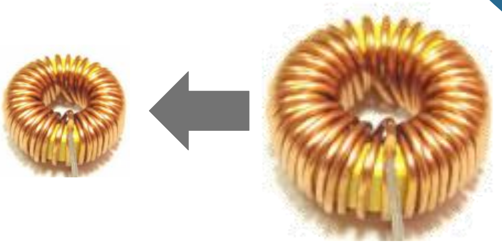
3Φ B6 Rectifier PFC (~70kHz)

FB LLC (150~400kHz)



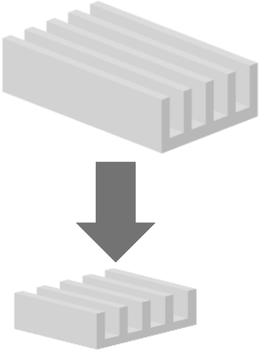
更高的开关频率

更小的被动器件



更小尺寸的散热器

更好的导热效果



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SiC MOSFET
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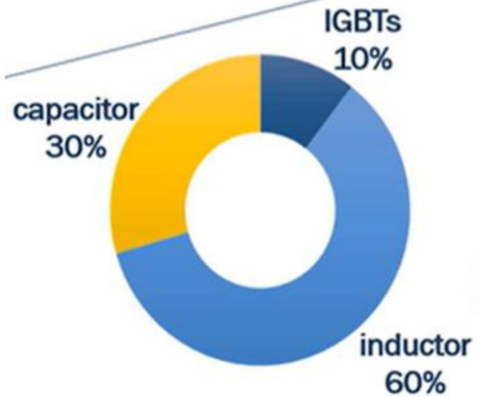
碳化硅方案系统级优势

- 小型化
- 轻质化
- 成本效益

Si vs SiC 30KW Inverter BOM

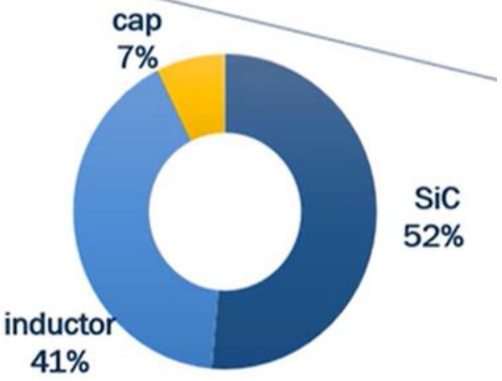


20KHz Si IGBT Solution

24 IGBTs	$ 48
Inductors	$ 276
Capacitors	$ 135
TOTAL BOM COST	$ 460

80KHz SiC MOSFET Solution

24 SiC MOSFET's	$ 230
Inductors(75% smaller in value)	$ 193
Caps (75% smaller in value)	$ 33
TOTAL BOM COST	~ $ 450



图片摘自https://www.onsemi.com/design/resources/video-library/utilizing-wide-bandgap-wbg-in-solar-and-renewable-energy-applications

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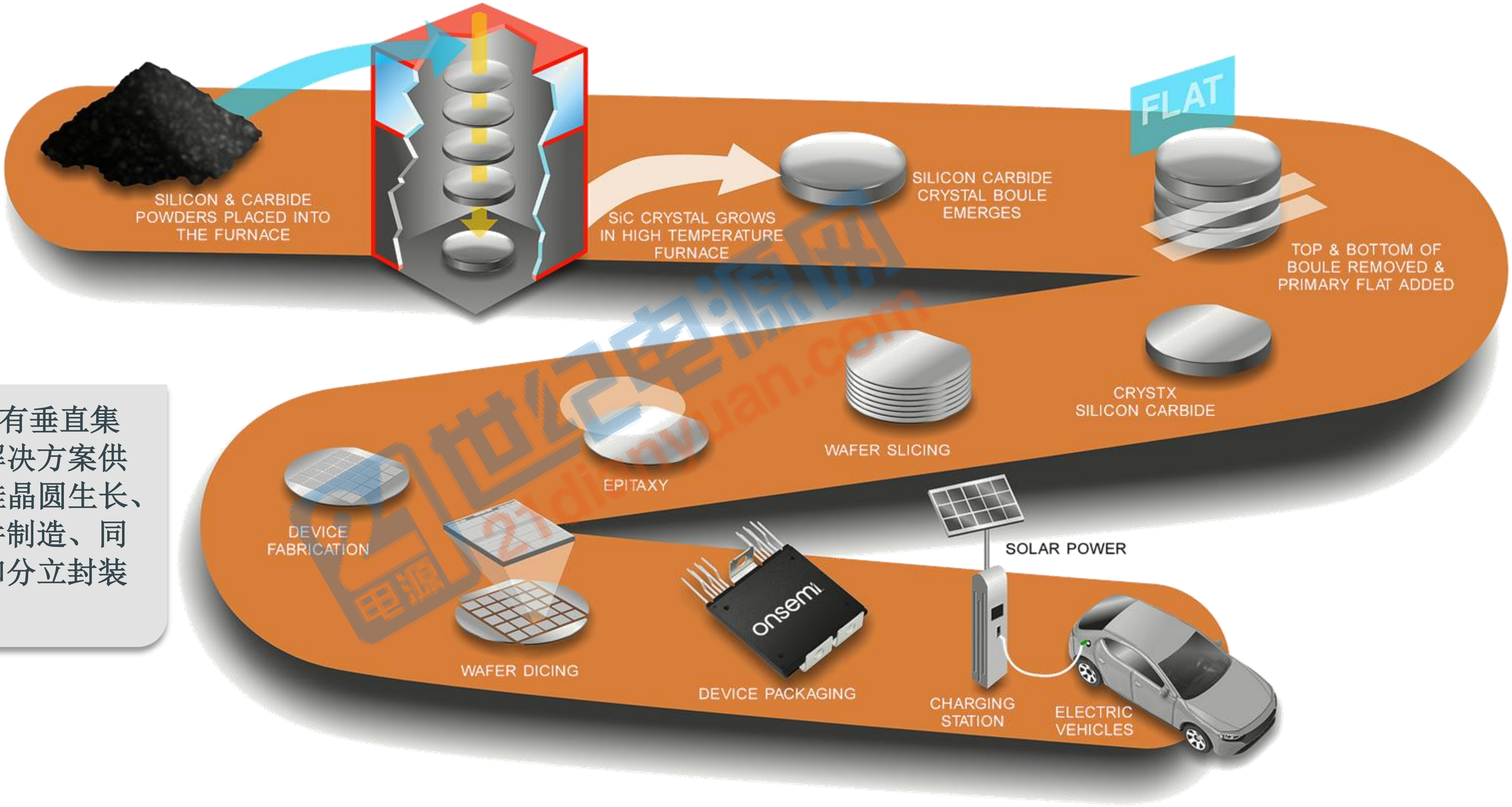
onsemi Silicon Carbide Manufacturing Life Cycle



onsemi 是一家具有垂直集成能力的碳化硅解决方案供应商，包括碳化硅晶圆生长、衬底、外延、器件制造、同类最佳集成模块和分立封装解决方案

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SiC MOSFET应用设计

碳化硅关键参数

参考资料：

https://www.onsemi.com/download/application-notes/pdf/and90103-d.pdf

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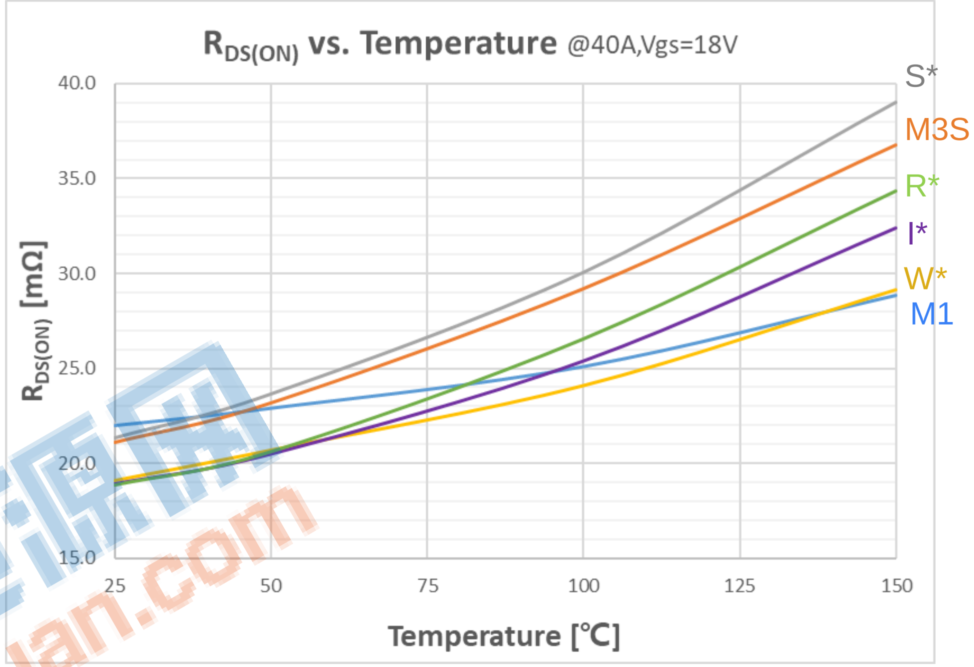
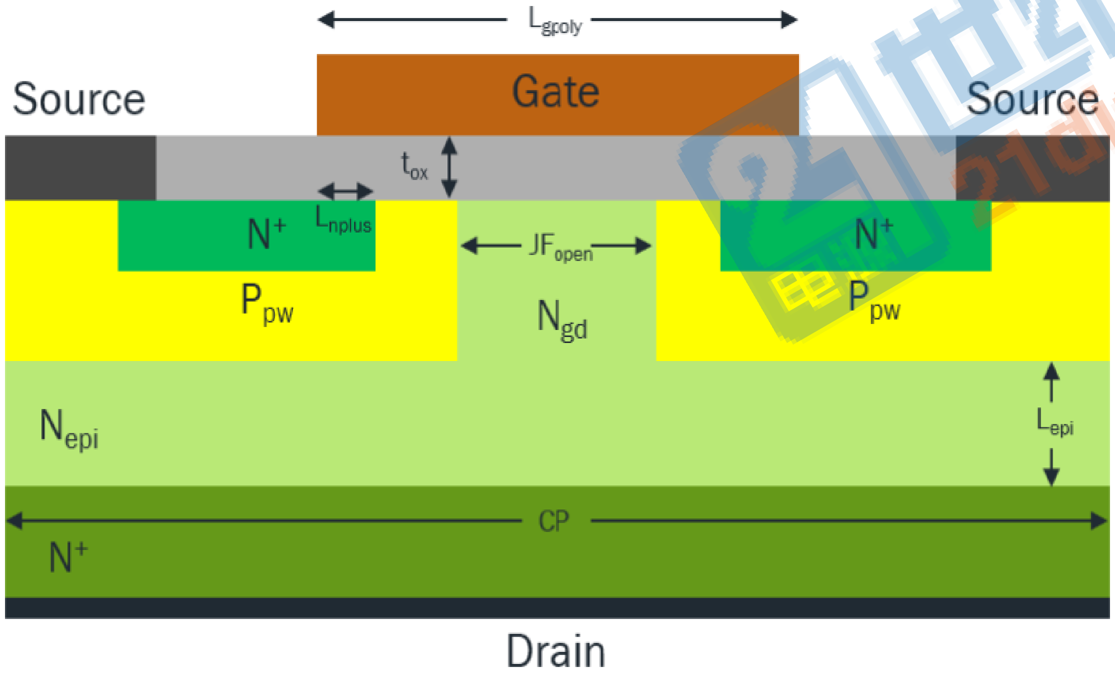
DOI：11.11985/2016.01.001

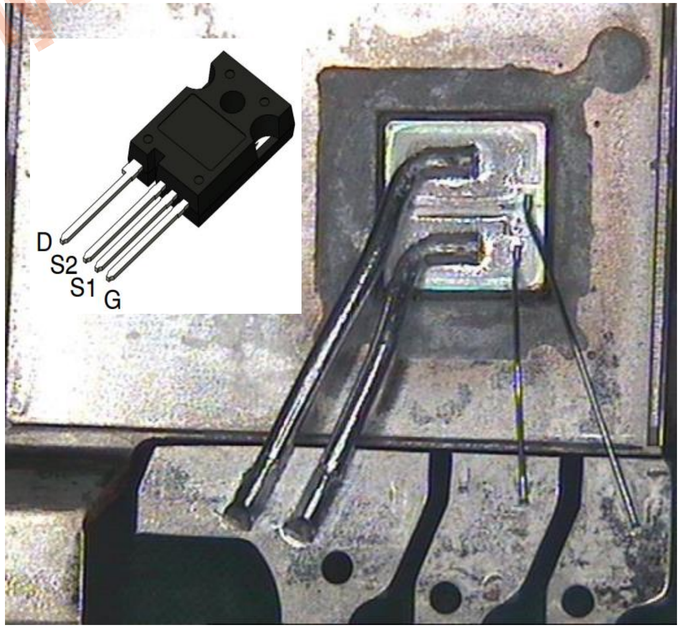
碳化硅MOSFET常见静态参数

Rds(on)温度系数

- 沟道电阻： NTC
- JFET区电阻：PTC
- 漂移区电阻：PTC







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$P\_loss = P\_cond + P\_sw$

光伏储能、EVC等高频开关应用中功率器件的开关损耗占主导→ M3S Win

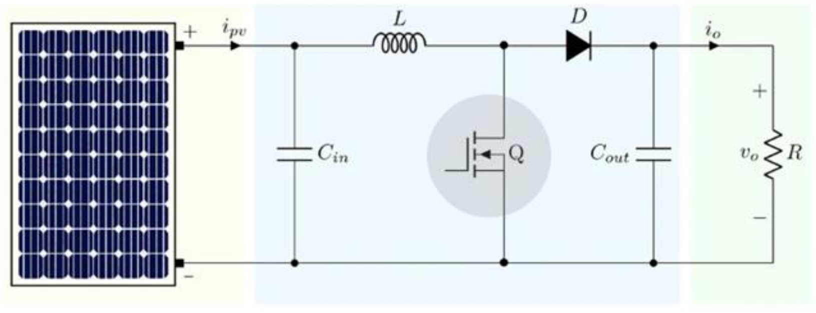
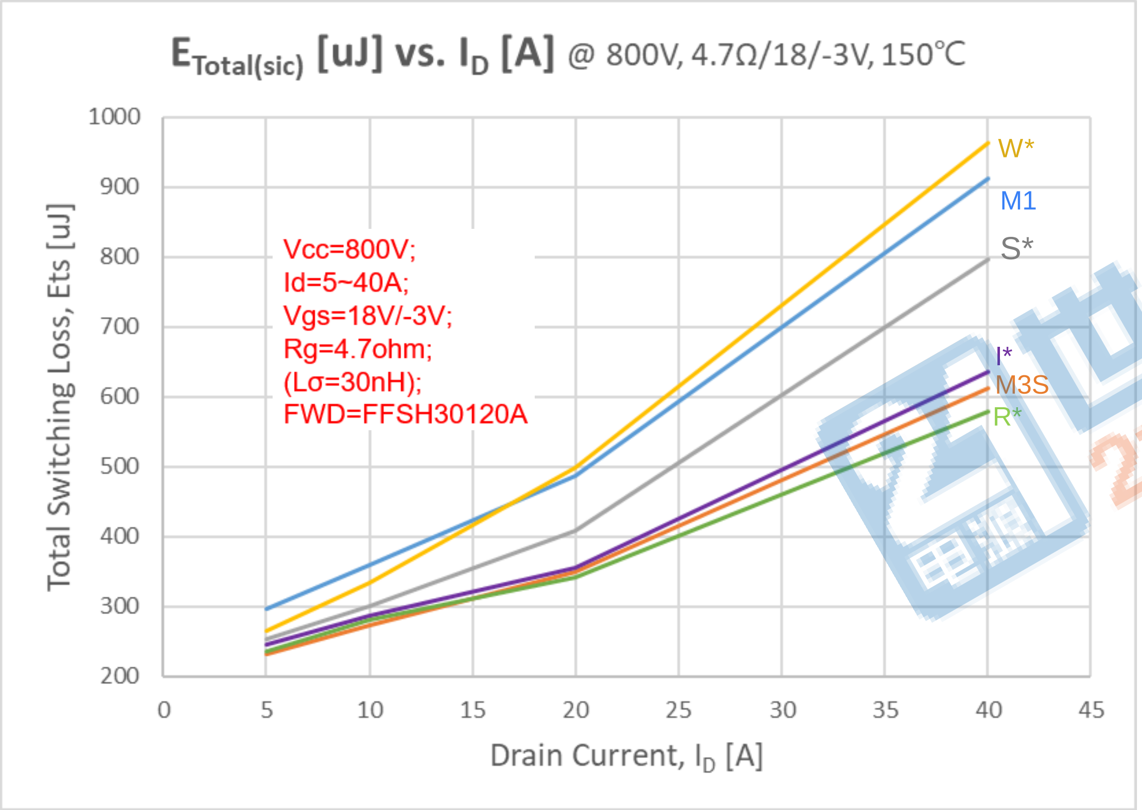
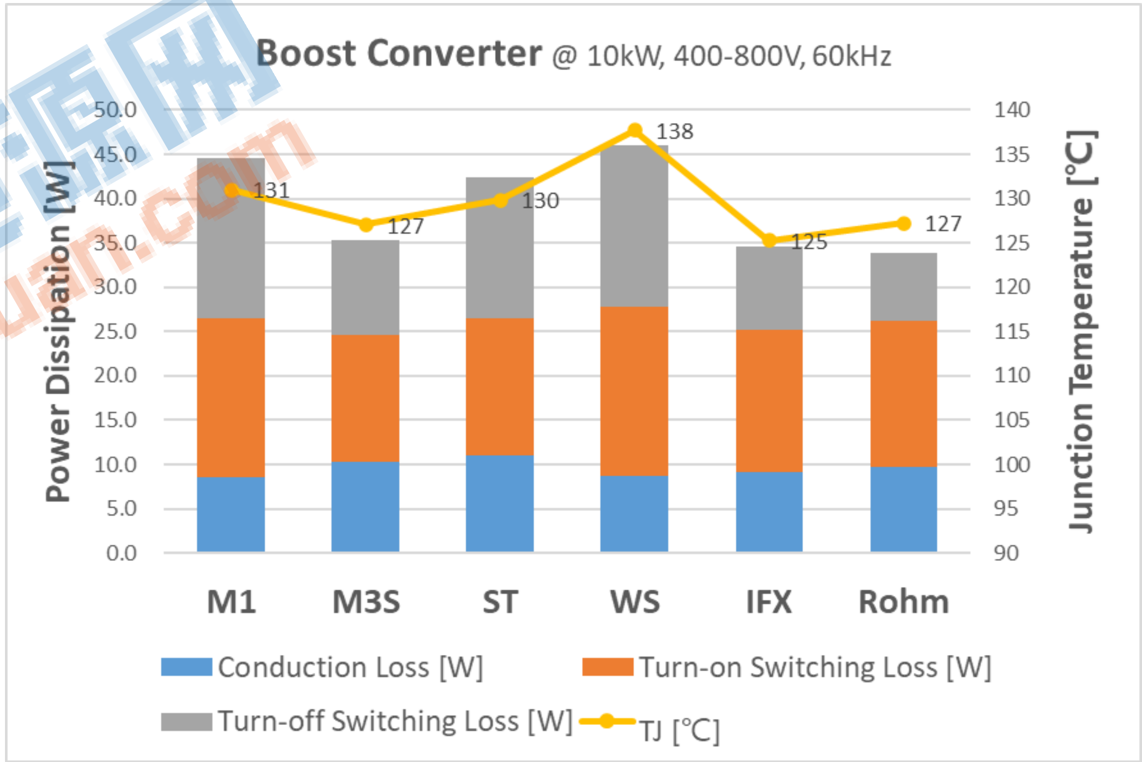


Image from https://latexdraw.com/draw-a-dc-dc-boost-converter-in-latex-using-circuitikz/



Vin=400V
Vo=800V
Po=10kW
fsw=60kHz
Vgs=-3/18V
Rg=4.7Ohm
FWD=SiC-SBD
Tsink=90 deg.C
Rthcs=0.62K/W
Rthjc=max in DS



碳化硅MOSFET常见静态参数

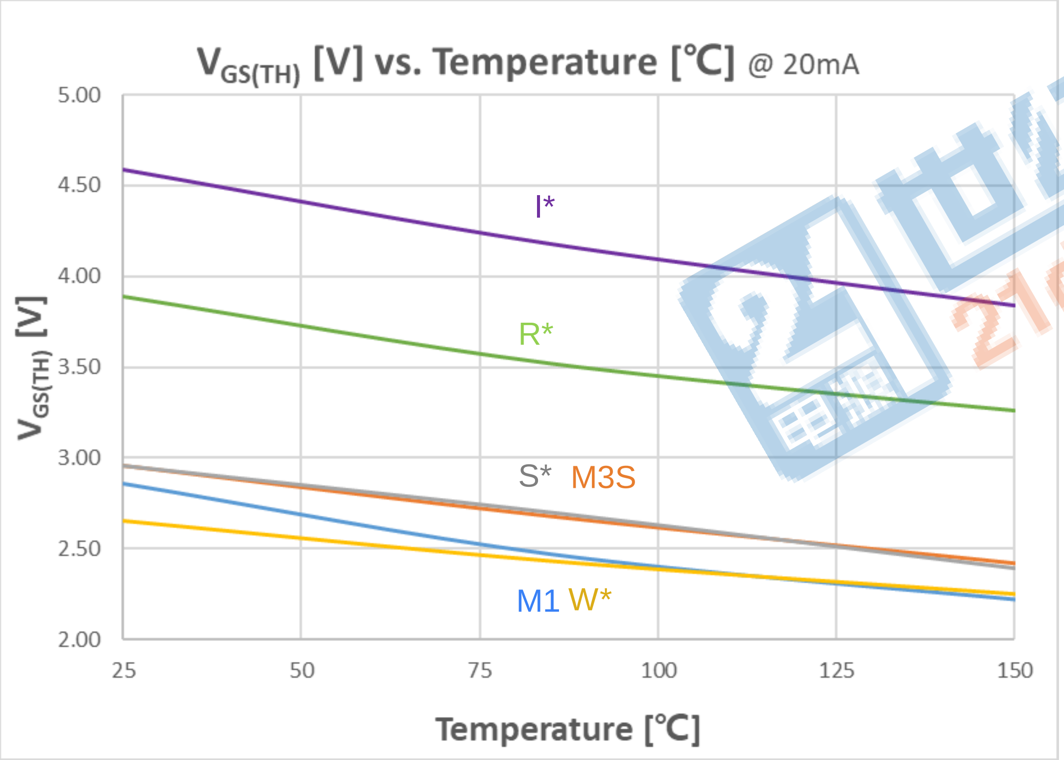
$V_{GS(TH)}$温度依赖性→NTC

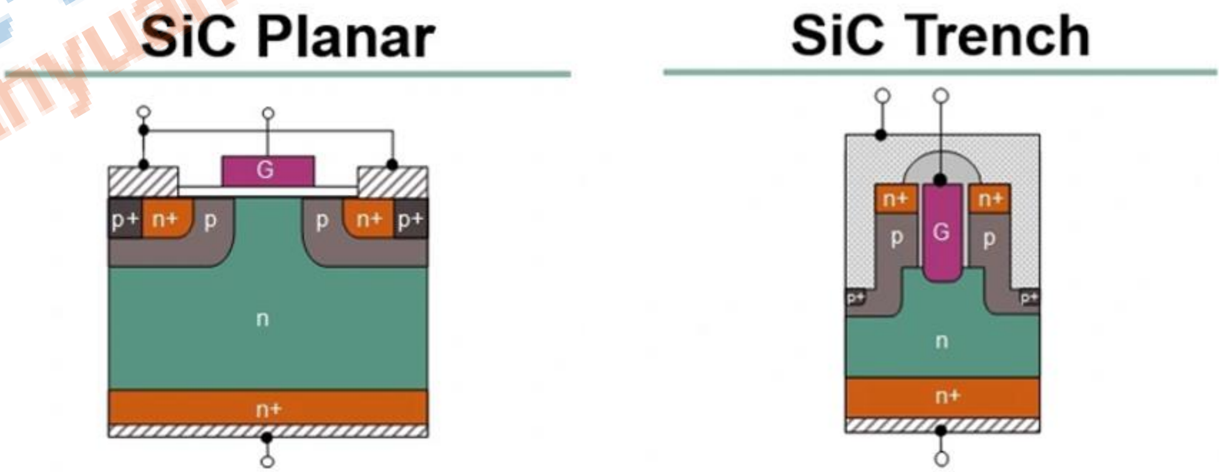
相同工艺水平下，栅极阈值电压越低则比导通电阻越小，即$V_{GS(TH)}$与R_{SP}呈正相关；

工艺限制

较低的$V_{GS(TH)}$会导致较差的抗噪声能力

- 米勒电容由dv/dt引起的感应电流尖峰导致误导通；
- 公共源极寄生电感由di/dt引起的感应电压尖峰导致误导通；
- 寄生电感与寄生电容之间的谐振振荡；





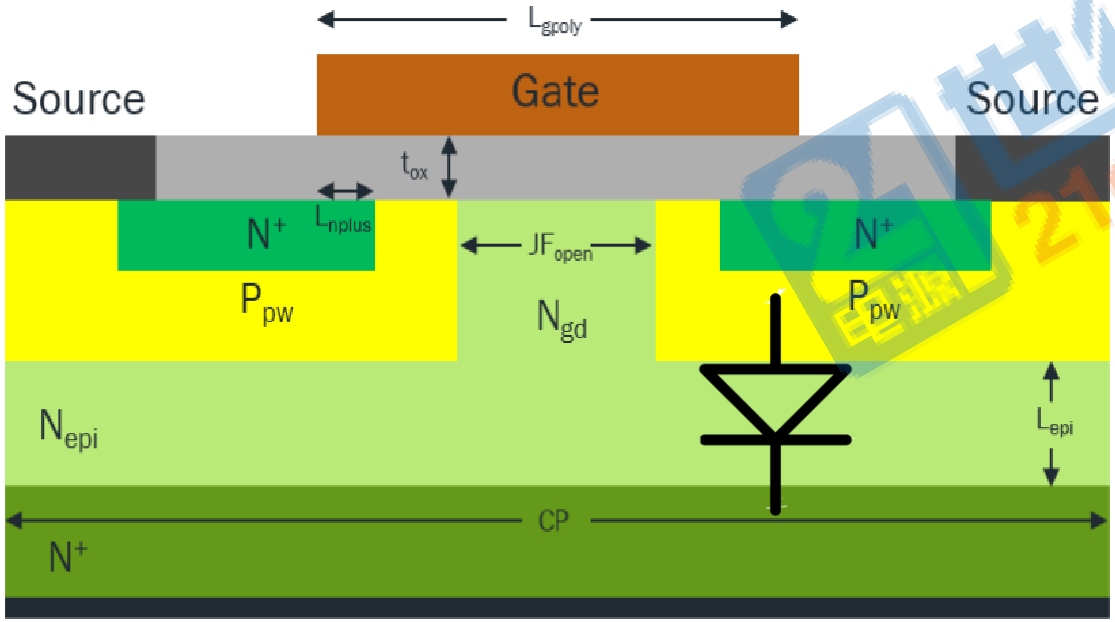
碳化硅MOSFET常见静态参数

VGS(OP)推荐栅源工作电压

- RDS(ON)→漏源导通电阻；
- EON、EOFF→开关损耗；
- VF→体二极管顺向压降；
- EREC→体二极管反相恢复损耗；
- 栅氧可靠性；

工艺限制

- 更高的VGS(OP)要求更大的额定值裕量；
- 栅氧层厚度加厚会降低沟道迁移率和跨导率、减慢开关速度；



Key Parameters @ conditions, RT		NTH4L040N120M3S	C3M0040120K
$V_{gs(op)}$ [V]		18V/-3V	15V/-4V
$V_{gs(max)}$ [V]		22V/-10V	19V/-8V
$R_{ds(on)}$ [mΩ]	@ Vgs=18V/15V; Id=30A;Tj=25℃	40	40
$R_{ds(on)}$ [mΩ]	@ Vgs=18V/15V; Id=30A;Tj=150℃	62	61
Q_g [nC]	@ 800V, 30A/40A, Vgs=18/-3V→onsemi; Vgs=15/-4V→Wolfspeed	107	118

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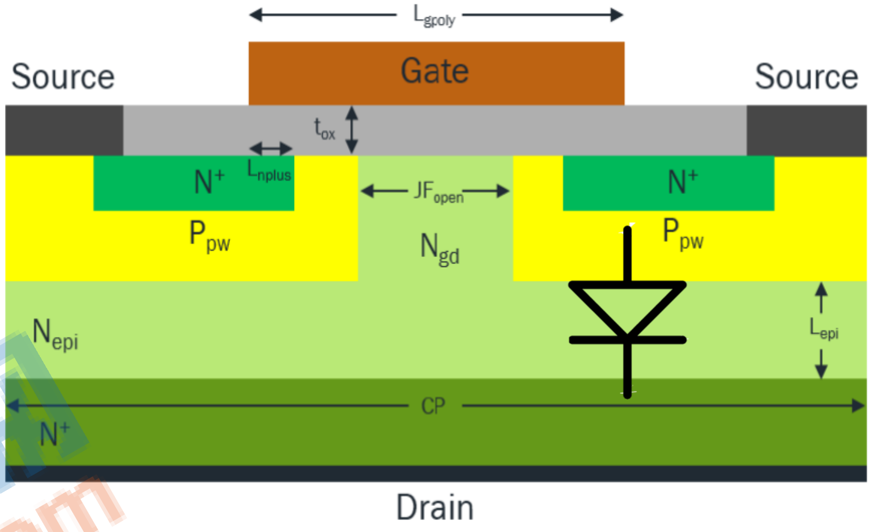
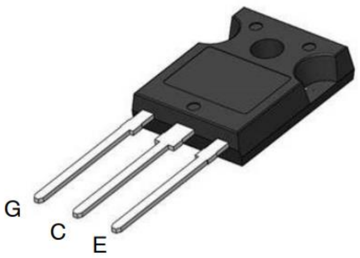
碳化硅MOSFET常见静态参数

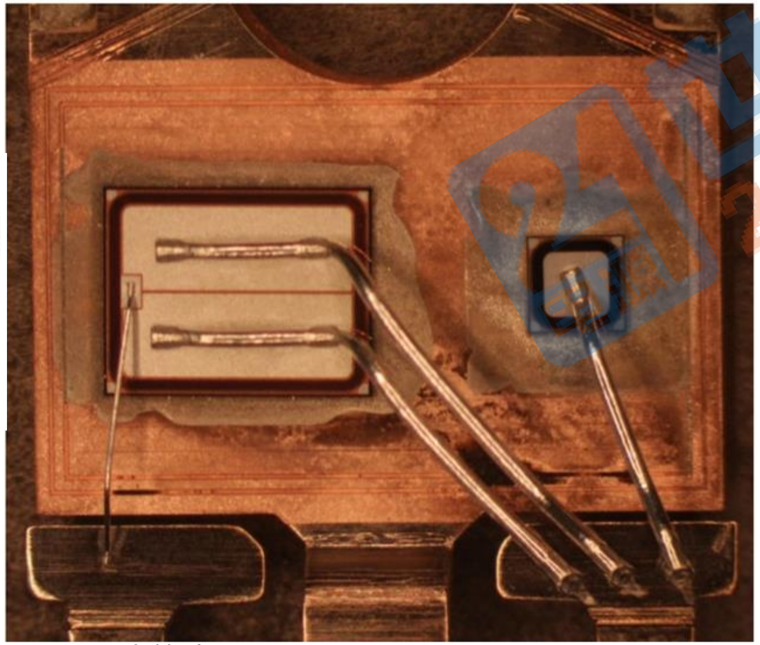
VF 体二极管导通压降

- NTC;
- VF更大相比硅 MOSFET体二极管;
- Erec更小相比硅 MOSFET体二极管;



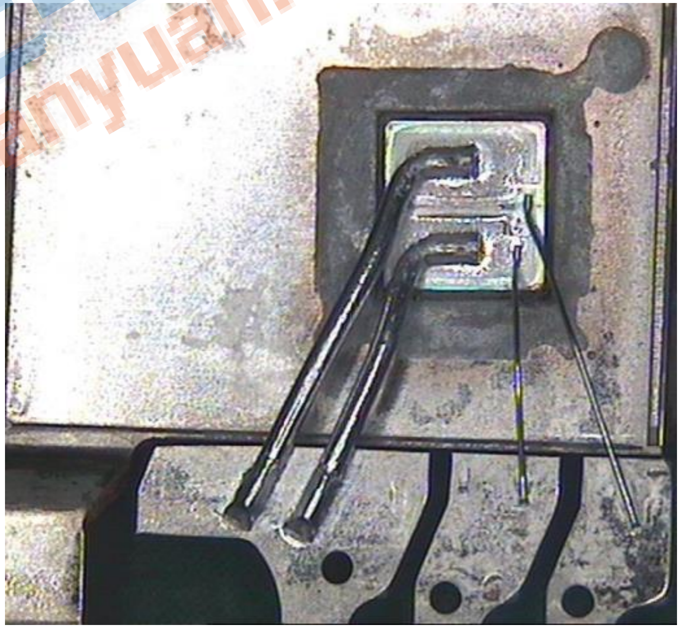
IGBT内部晶圆



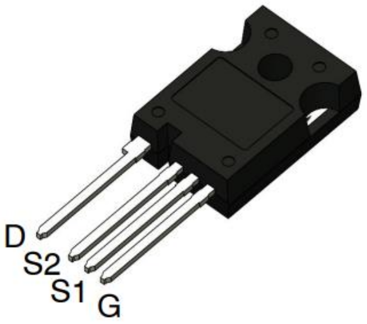


图片摘自www.onsemi.com-AND9140-D

SiC MOSFET内部晶圆



SiC MOSFET破坏性测试光学图片



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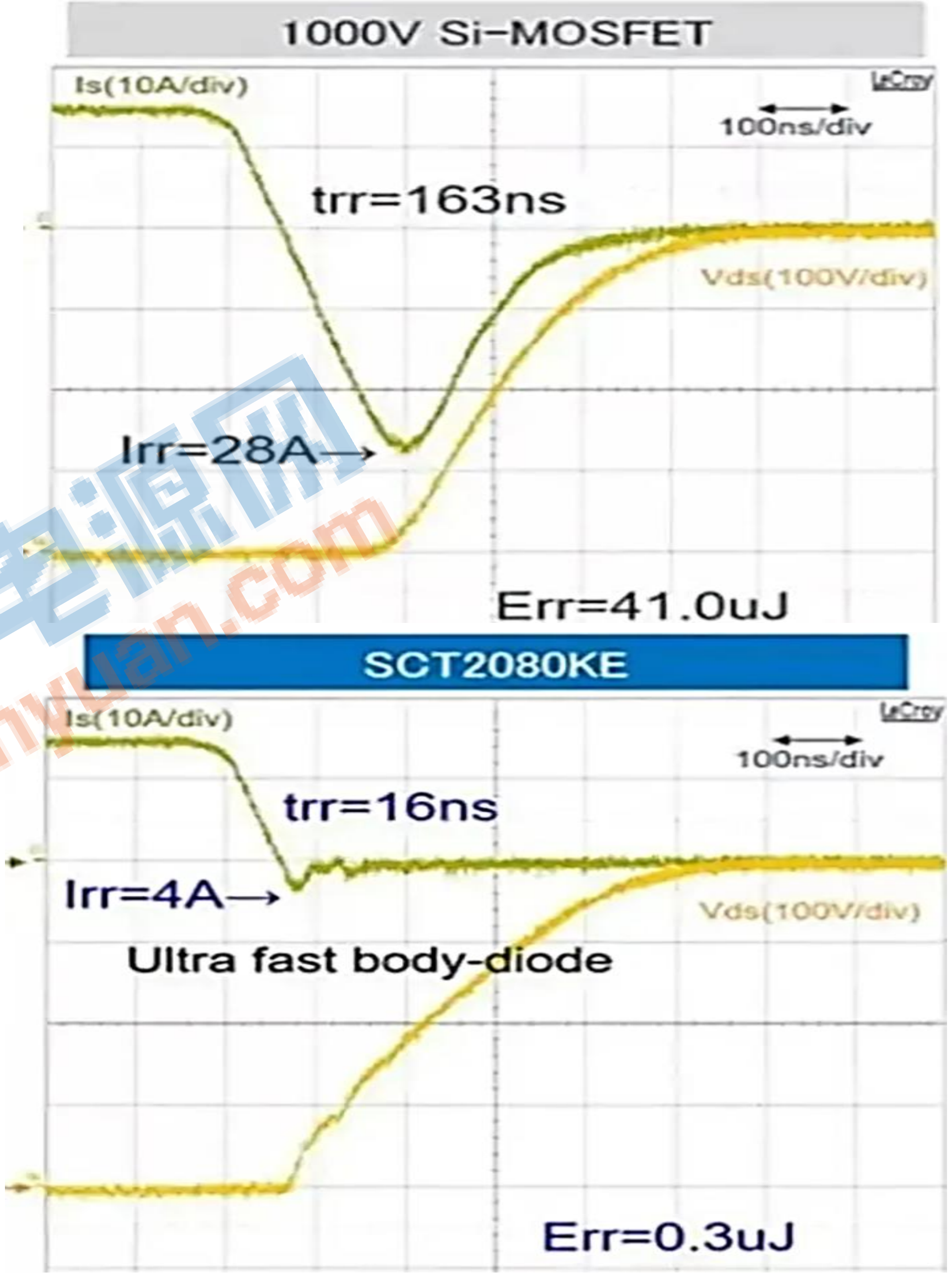
碳化硅MOSFET体二极管导通压降

类别	VF导通压降 typical@25℃
硅 PN 结二极管	1.5 V ~ 3 V
碳化硅 SBD	1.38 V ~ 1.75 V
C3M0032120K	4.2 V ~ 4.6 V
IMZA120R030M1H	3.6 V ~ 5.0 V
NTH4L030N120M3S	4.6 V
IGBT体二极管	1.5 V ~ 2 V
IGBT SiC SBD	1.45 V ~ 1.80 V

SCT2080KE Datasheet

●**Body diode electrical characteristics** (Source-Drain) (T_a = 25°C)

Parameter	Symbol	Conditions	Values			Unit
			Min.	Typ.	Max.	
Body diode continuous, forward current	I_S *1	T_c = 25°C	-	-	40	A
Body diode direct current, pulsed	I_{SM} *2	T_c = 25°C	-	-	80	A
Forward voltage	V_{SD} *4	V_{GS} = 0V, I_S = 10A	-	4.6	-	V
Reverse recovery time	t_{rr} *4	I_F = 10A, V_R = 400V di/dt = 150A/μs	-	31	-	ns
Reverse recovery charge	Q_{rr} *4	I_F = 10A, V_R = 400V di/dt = 150A/μs	-	44	-	nC
Peak reverse recovery current	I_{rrm} *4	I_F = 10A, V_R = 400V di/dt = 150A/μs	-	2.3	-	A



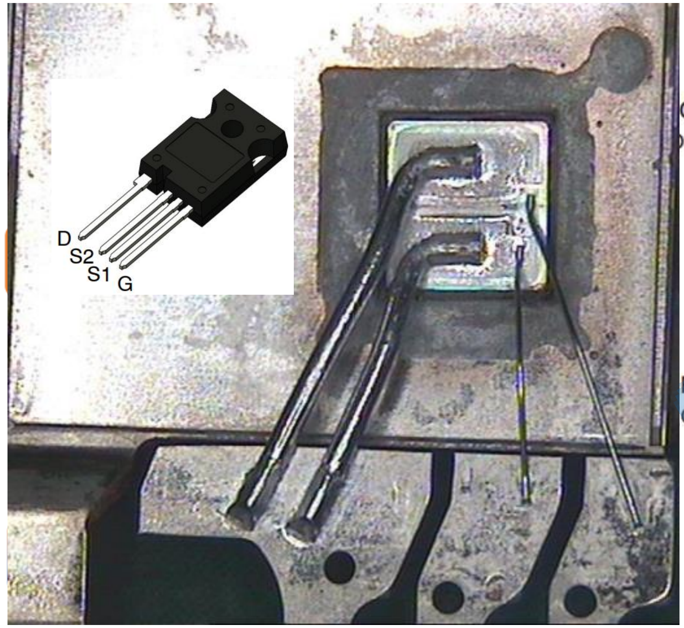
https://zhuanlan.zhihu.com/p/573910994

碳化硅MOSFET关键参数

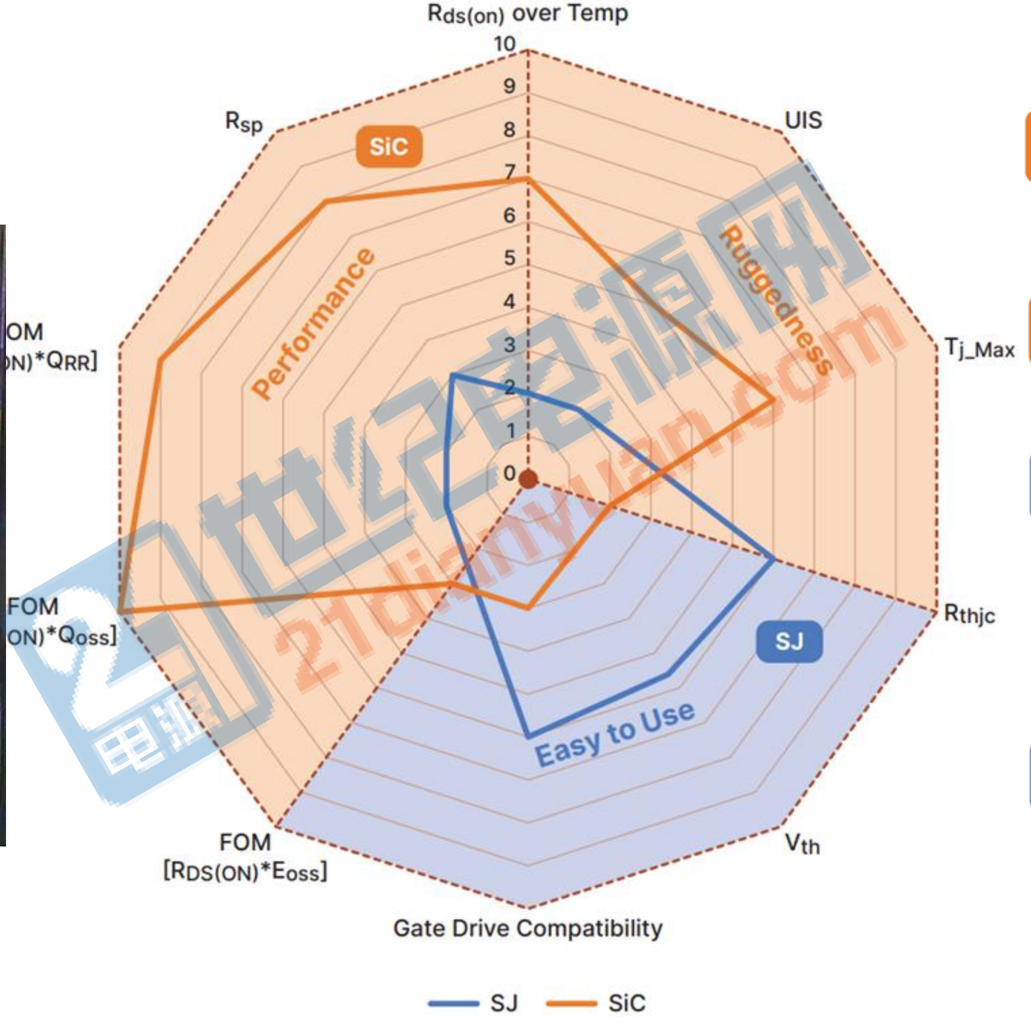
$R = \rho \times L \div S$

$Rsp = Rds \times S$

Rsp
- Lower value is better
- Winner: SiC
- SJ Tech is limited by Si



$Eoss = Qoss \times Vds$



RDS(ON) over Temp
- Lower value is better for Pcon@high T
- Winner: SiC
- SJ is limited by Si material

UIS
- Higher value is better
- Winner: SiC

Rthjc
- Lower value is better
- Winner: SJ
- Larger die size of SJ

Vth
- Higher value is better for immunity
- Winner: SJ
- Related false turn-on → Increasing Ploss and failure

Gate Drive Compatibility
- Gate drive voltage
- Winner: SJ (0 to 12 V)
- SiC (-5 to 18 V/0 to 18 V)

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SiC MOSFET应用设计

SiC MOSFET并联影响与栅极电阻设置

参考资料：

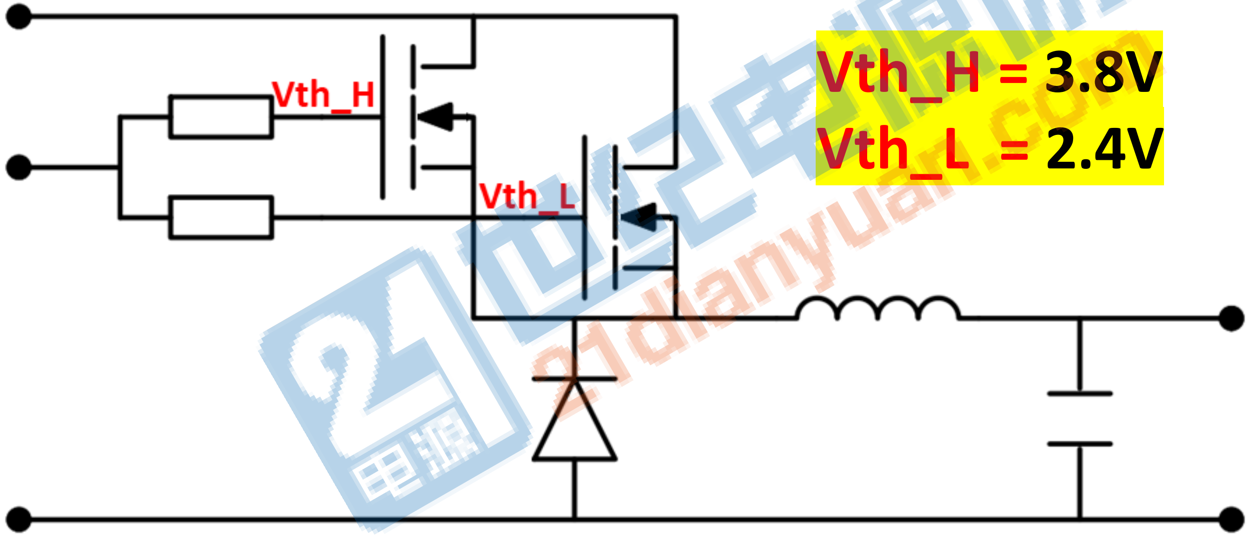
https://www.onsemi.com/download/application-notes/pdf/and90103-d.pdf;

TND6440 - Paralleling SiC MOSFETs Process Impacts and Gate Resistors Setup (onsemi.com);

https://ieeexplore.ieee.org/document/7931077/;

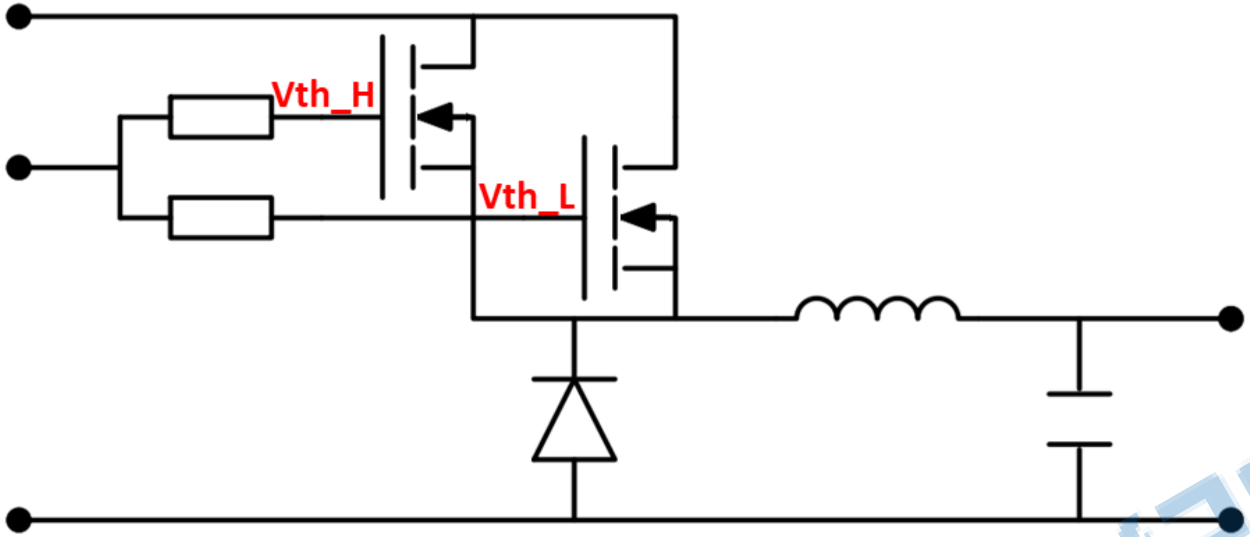
https://www.onsemi.com/download/application-notes/pdf/and90255-d.pdf;

工艺参数(Vth)不一致的SiC MOSFET并联会发生什么？



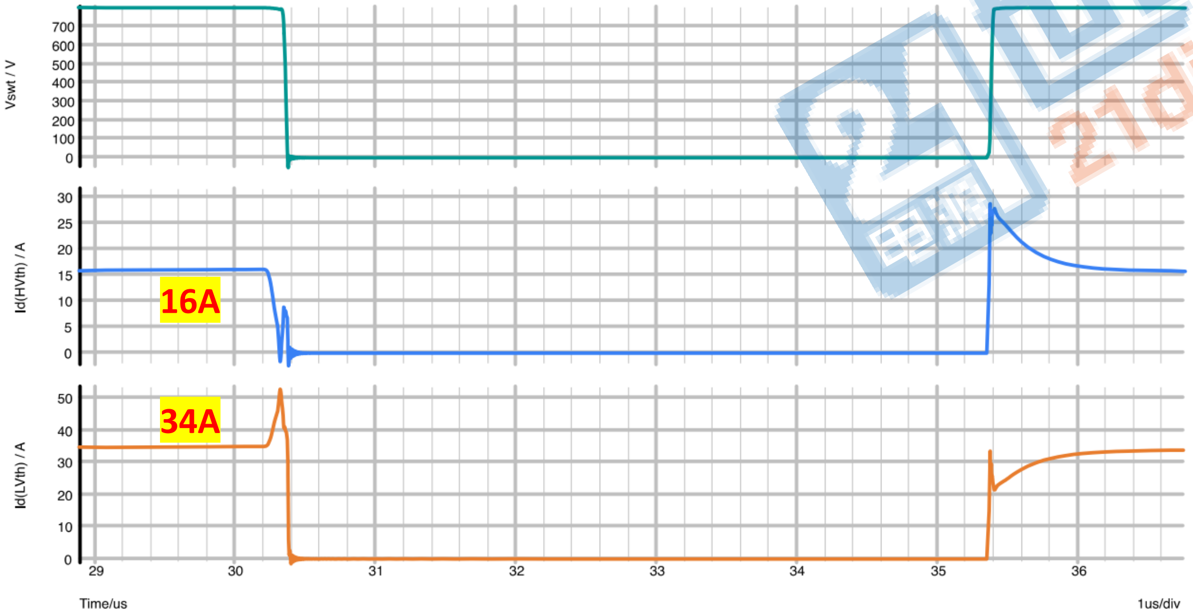
20KW降压电路

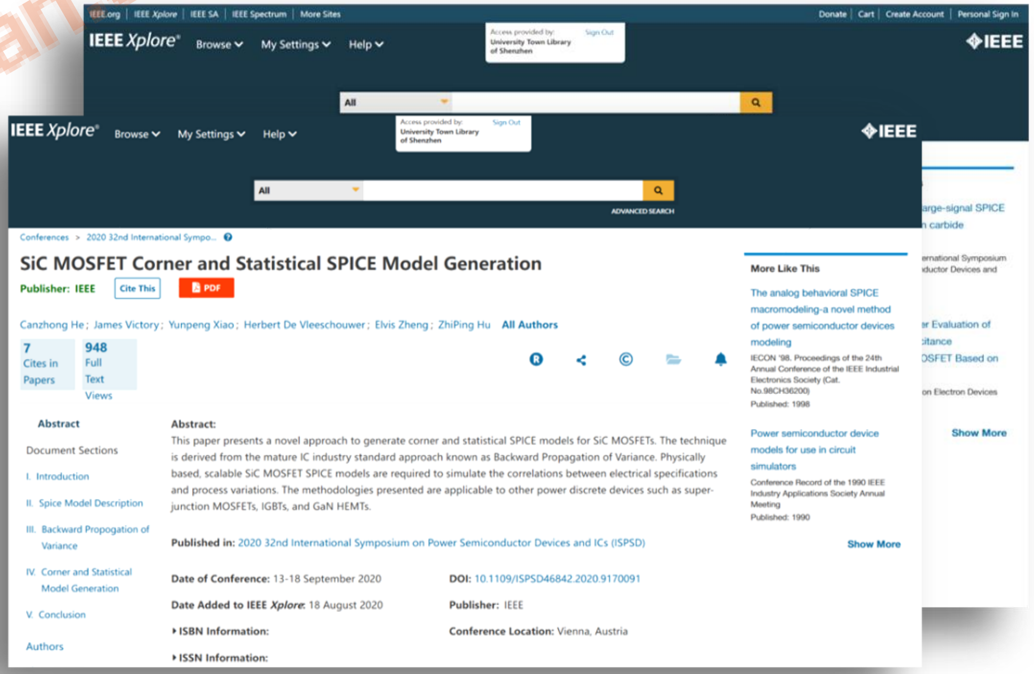
SiC MOSFET并联影响与栅极电阻设置



20KW降压电路

Vi = 800V
Vo = 400V
Rg = 10Ω
Fsw = 100KHz
Vth_H = 3.8V
Vth_L = 2.4V





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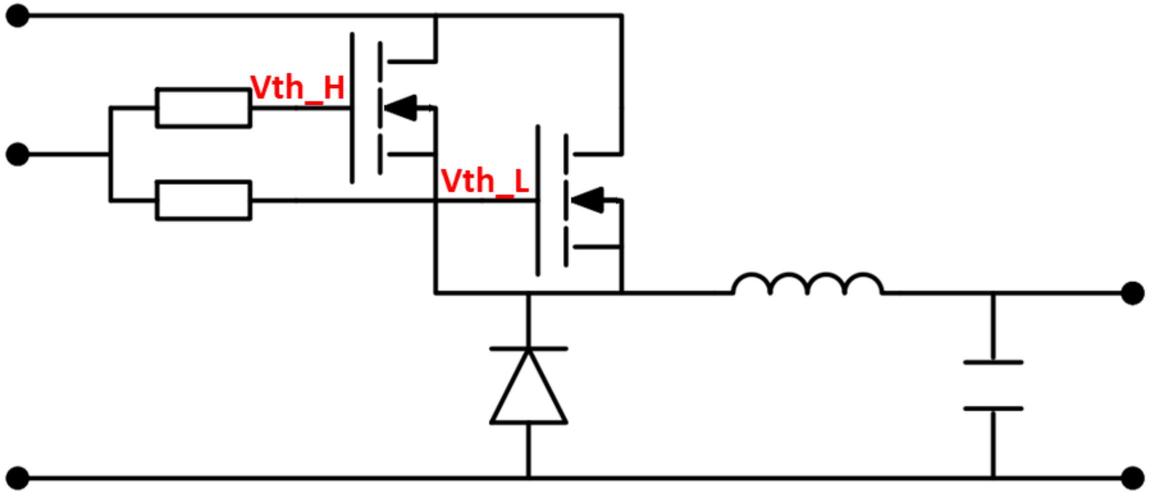
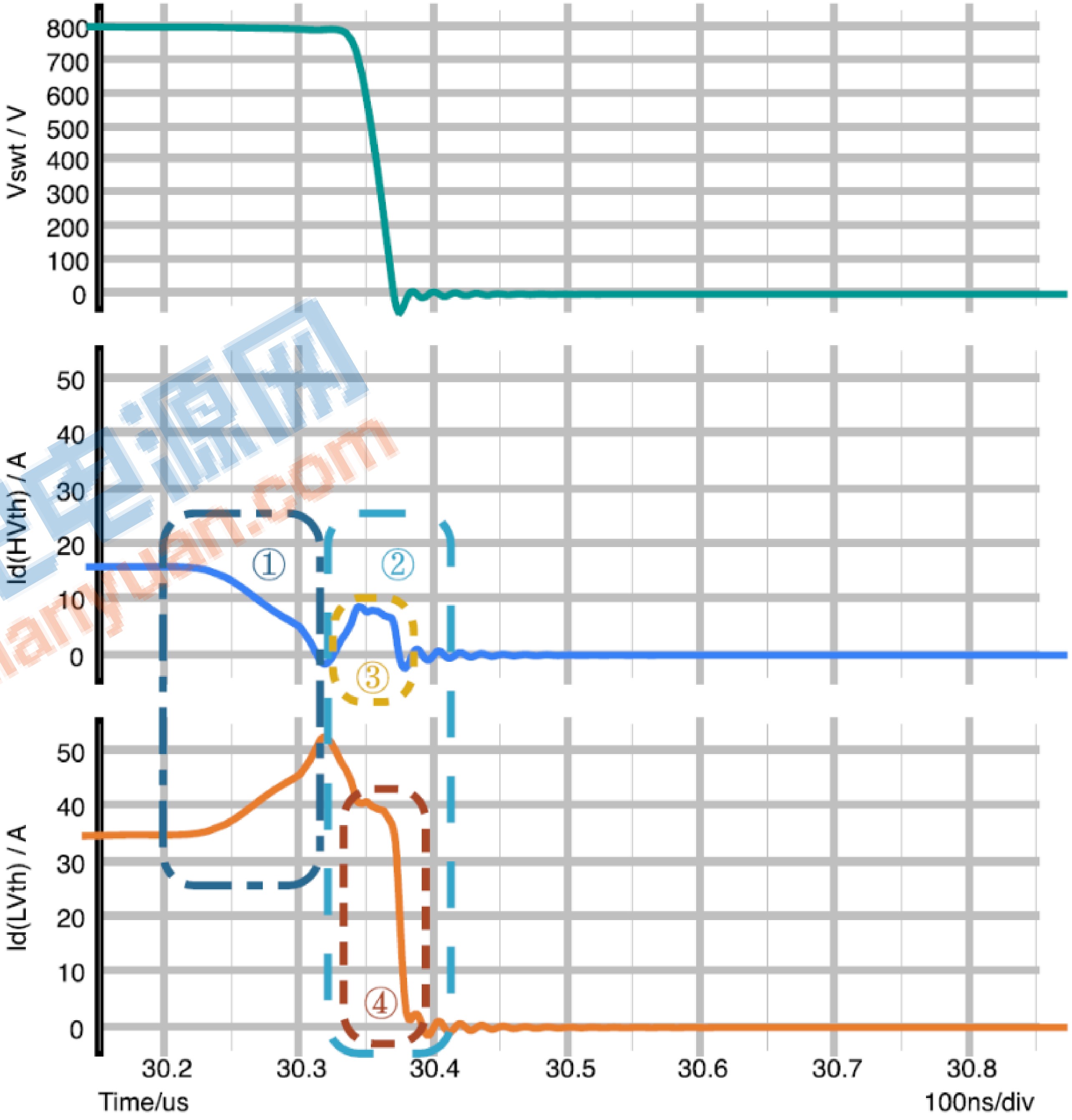
关断电流波形

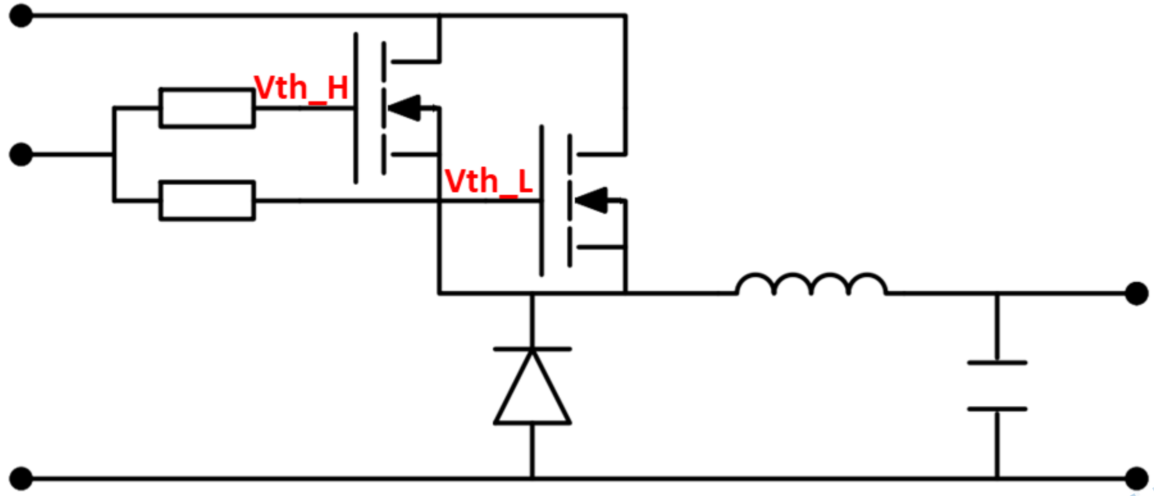


20KW降压电路

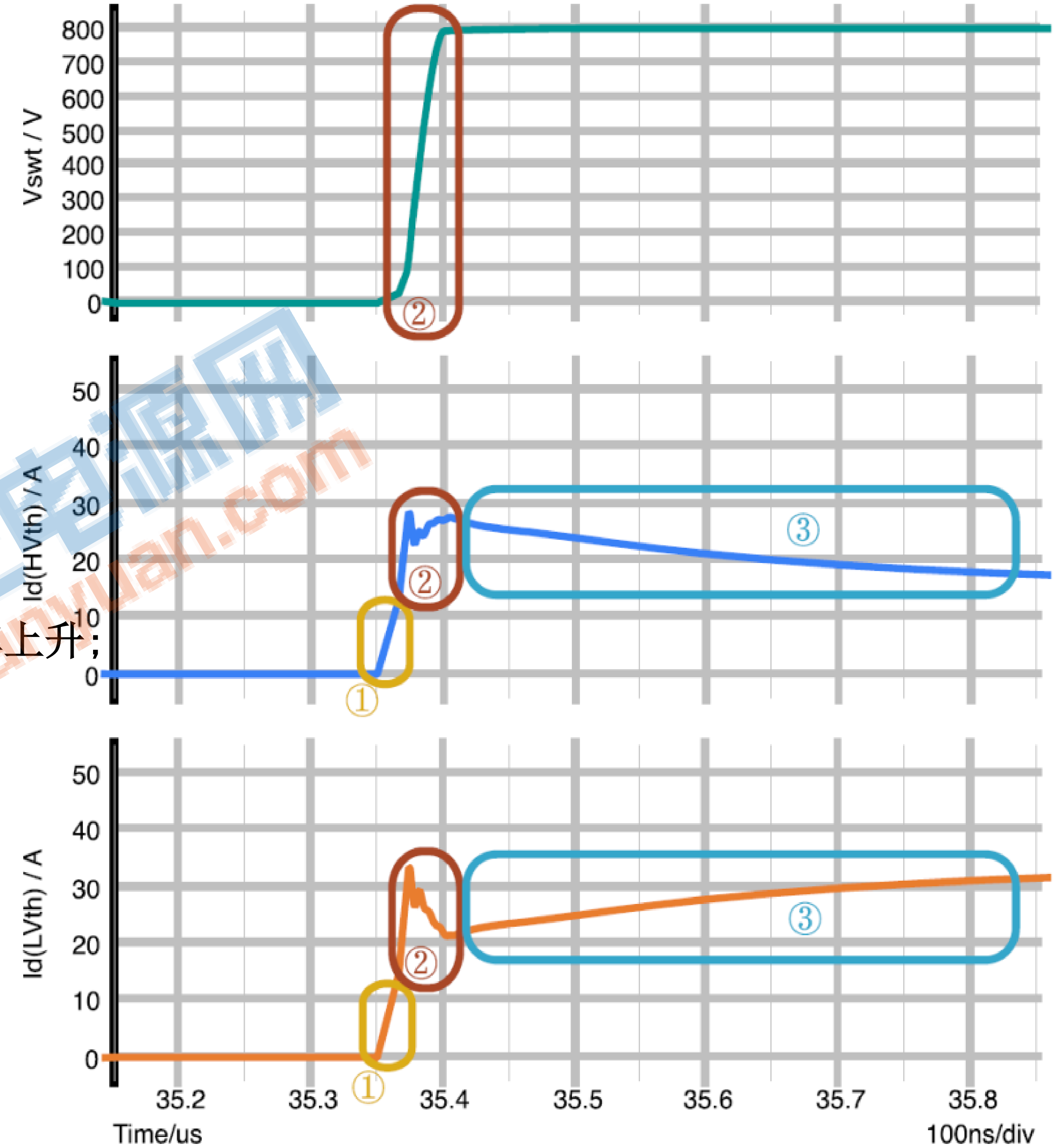


- ①Vth_H器件先关断，电流全部转移到Vth_L器件；
- ②Vth_L器件延迟关断；
- Vth_H器件Cds结电容充电引起电流尖峰；
- ③Id电流变化发生在开关节点过渡期间；
- ④Vth_L器件Cds充电电流与逐渐减小的漏极电流混合；

开通电流波形



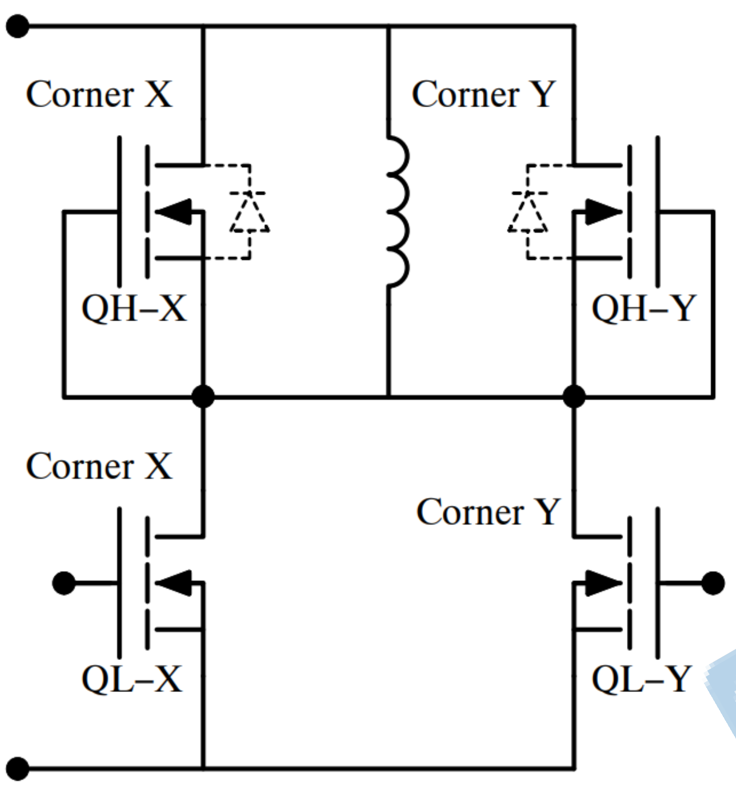
20KW降压电路



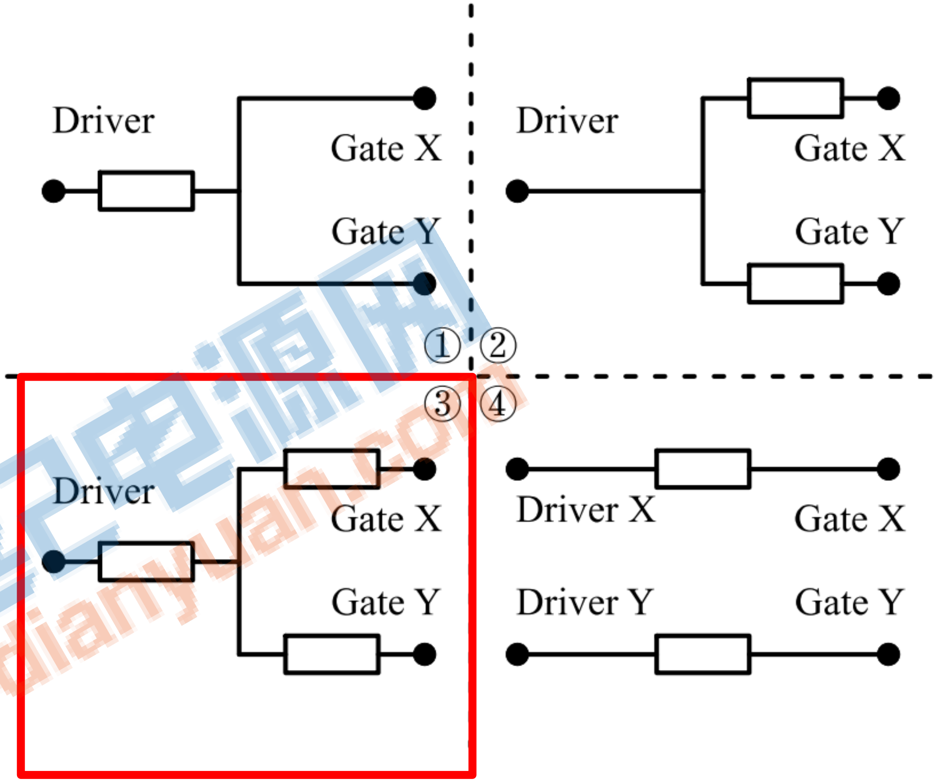
- ①在到达密勒平台之前两器件导通电流以大致相同的斜率上升；
- ②进入密勒平台，时间等于开关节点电压过渡时间；尖峰由SBD截至寄生结电容充访电电流引起；
- ③Vgs的继续增加，并联器件Rds(on)进入可变电阻区；

Case	Eon	Eoff	Peak Current before Miller Plateau	Peak Current after Miller Plateau	Current during ON–Time	Total Losses
LVth	380 µJ	650 µJ	33.5 A	28 A	34 A	105 W
HVth	350 µJ	100 µJ	28.5 A	22 A	16 A	45 W

DPT平台-改变栅极电阻



Vbus = 800V
IL = 100A
Vth_H = 3.8V
Vth_L = 2.4V

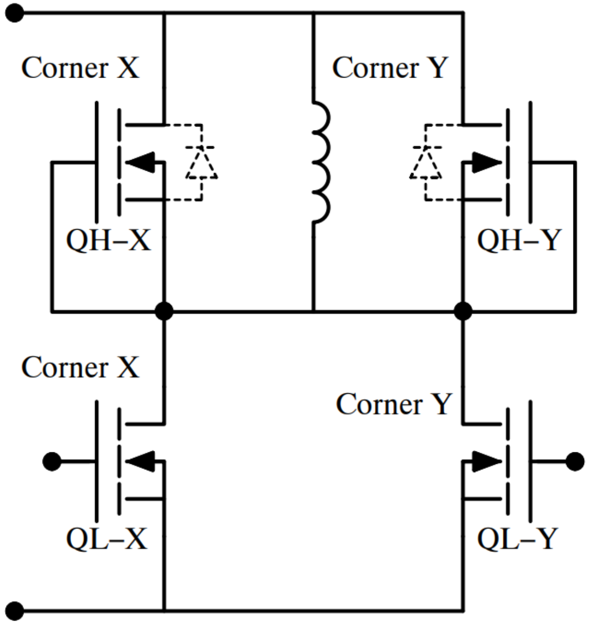


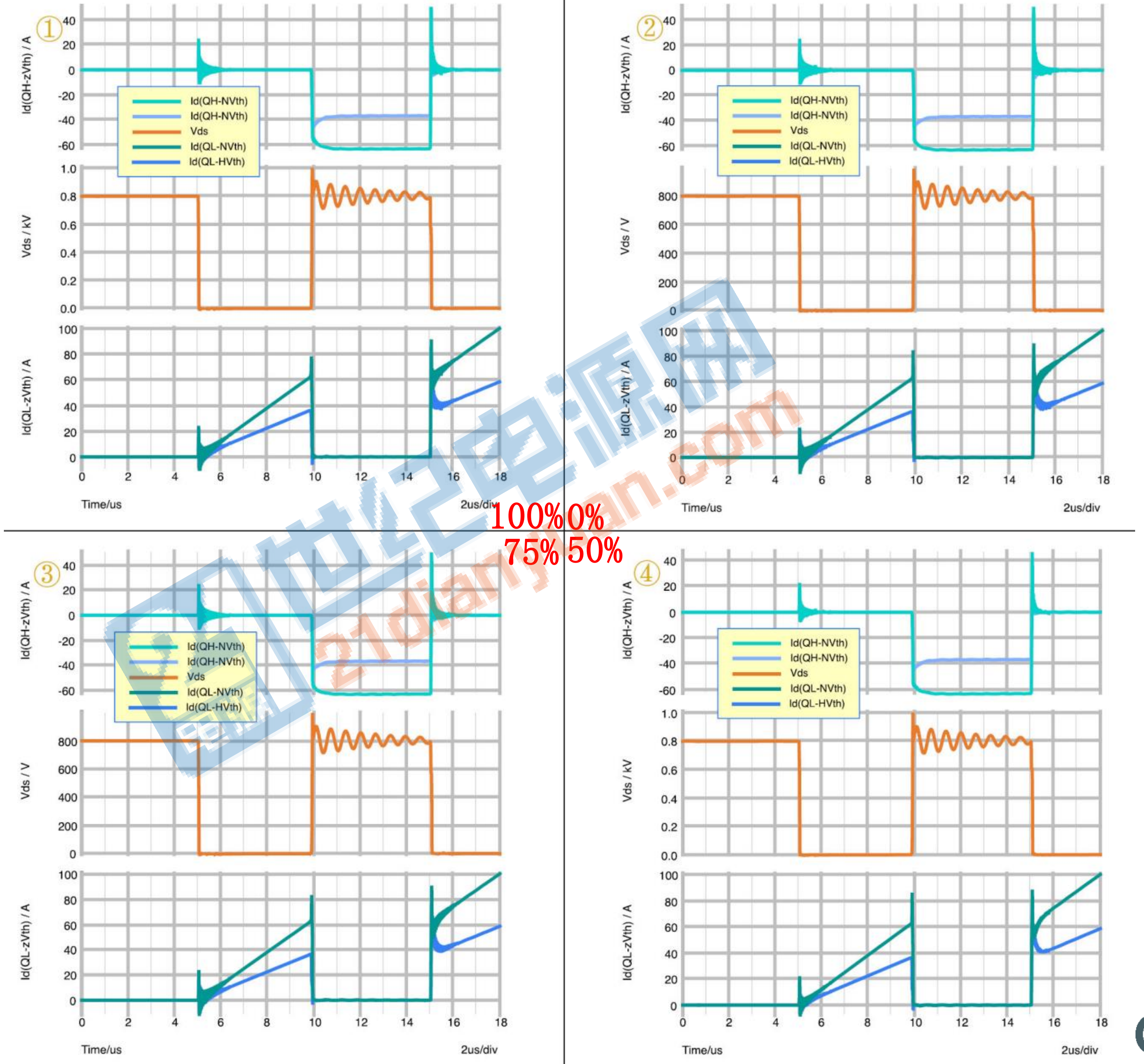
实现0%~100%的栅极分流比率；

0% →只有公共电阻；

100% →只有栅极电阻，无公共电阻

DPT测试结果





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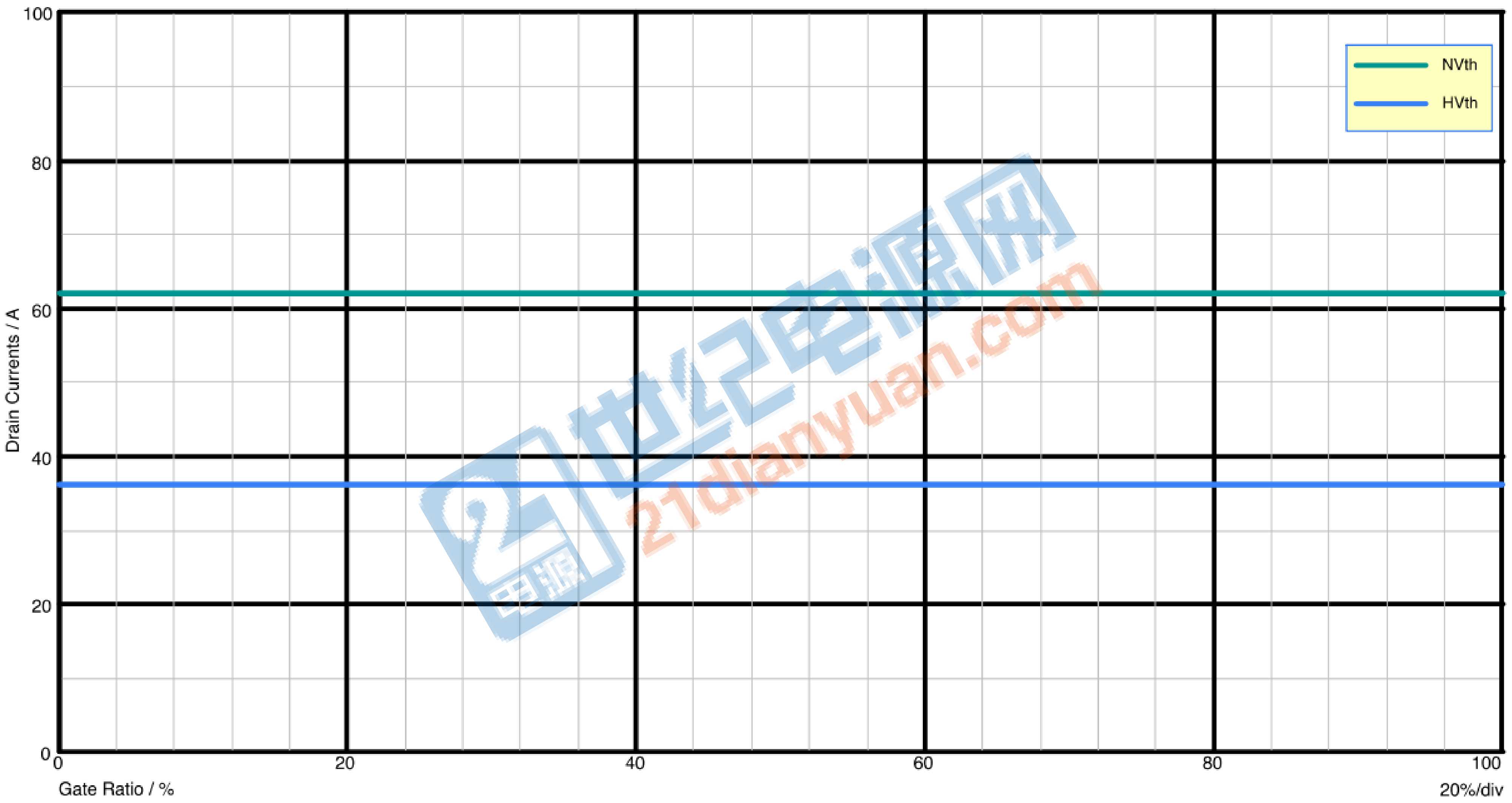
栅极电流



100
80
60
40
20
0
Drain Currents / A
0
20
40
60
80
100
Gate Ratio / %
20%/div
NVth
HVth

开关损耗

SiC VS. Si

- Vth导致的并联器件的不均流不受栅极电阻器配置的影响！
- 需要通过DPT根据实际工况测试对器件的一致性进行筛选排序再做并联设计；

SiC MOSFET应用设计

Vgs=0V驱动设计

参考资料：

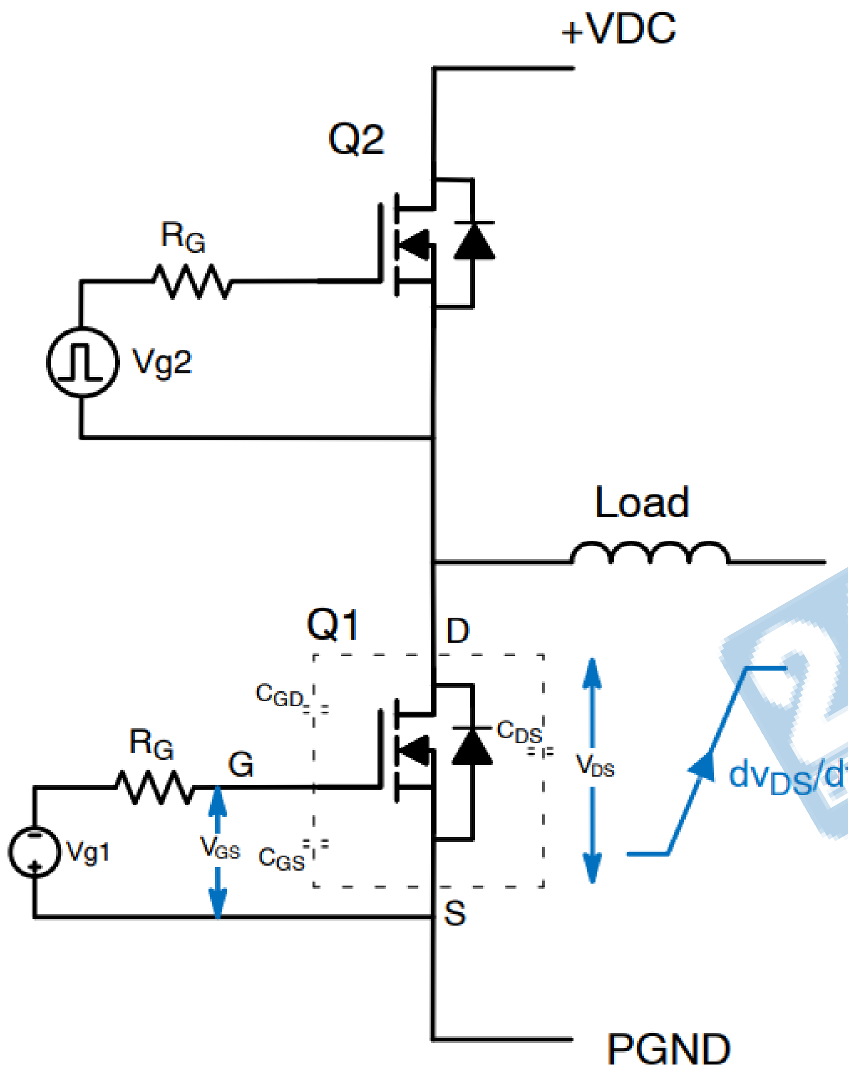
https://www.onsemi.com/download/application-notes/pdf/and90103-d.pdf;

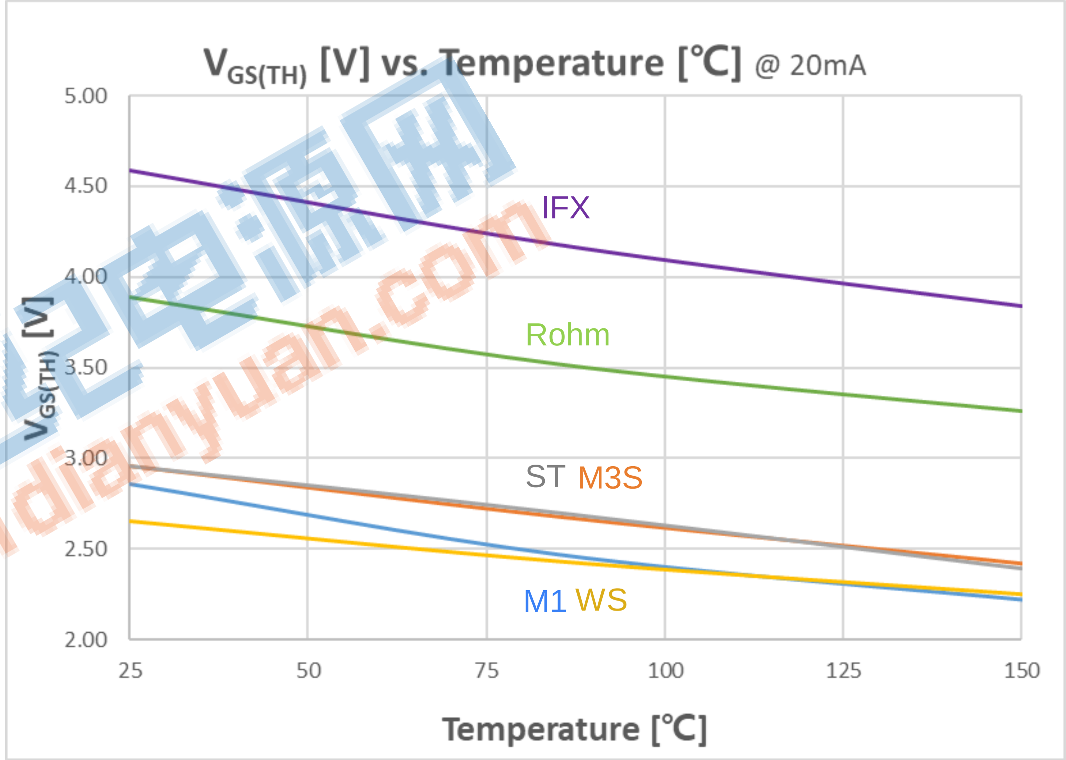
TND6440 - Paralleling SiC MOSFETs Process Impacts and Gate Resistors Setup (onsemi.com);

https://ieeexplore.ieee.org/document/7931077/;

https://www.onsemi.com/download/application-notes/pdf/and90255-d.pdf;

SiC MOSFET开关等效电路





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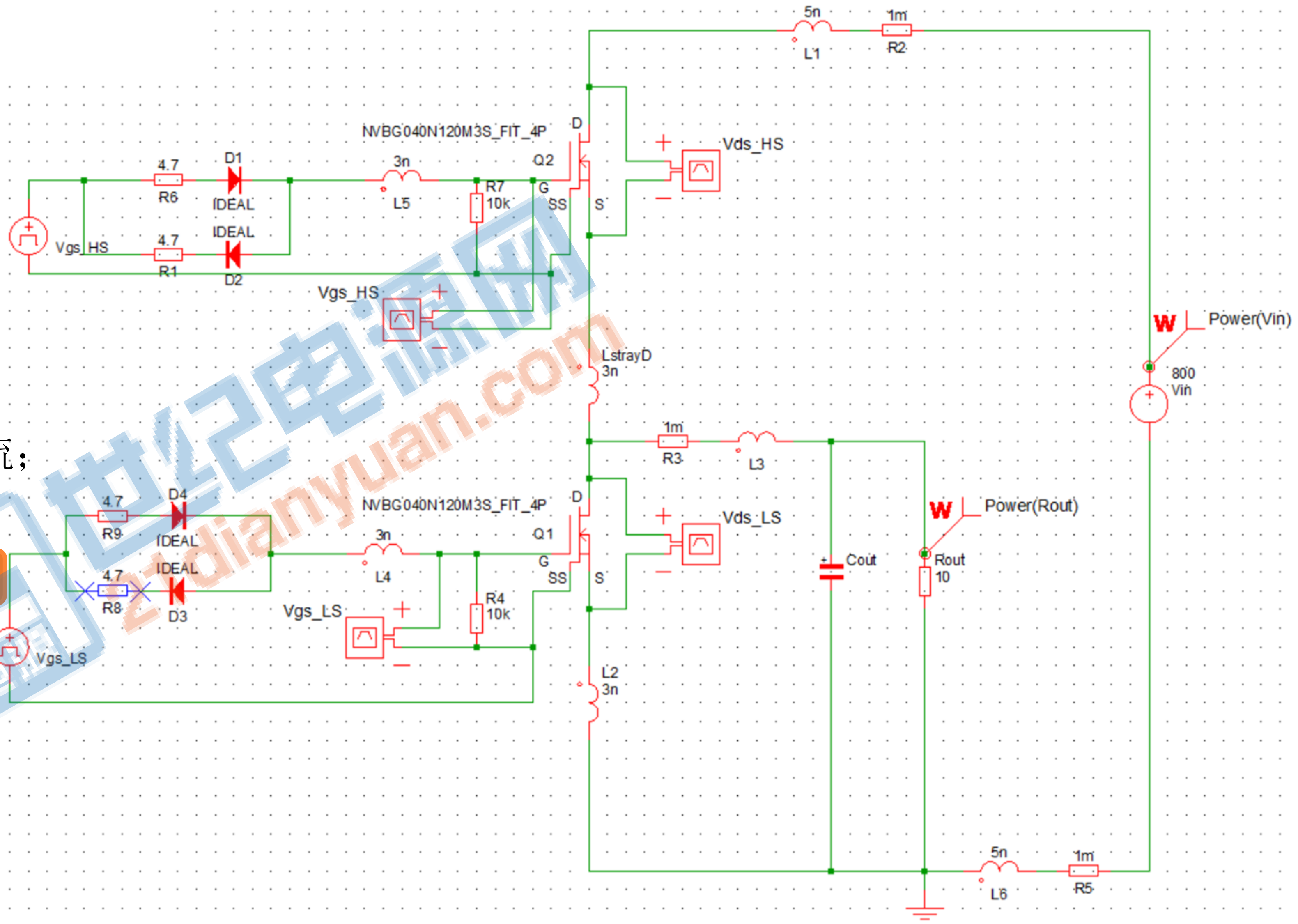
Simetrix仿真电路

测试数据

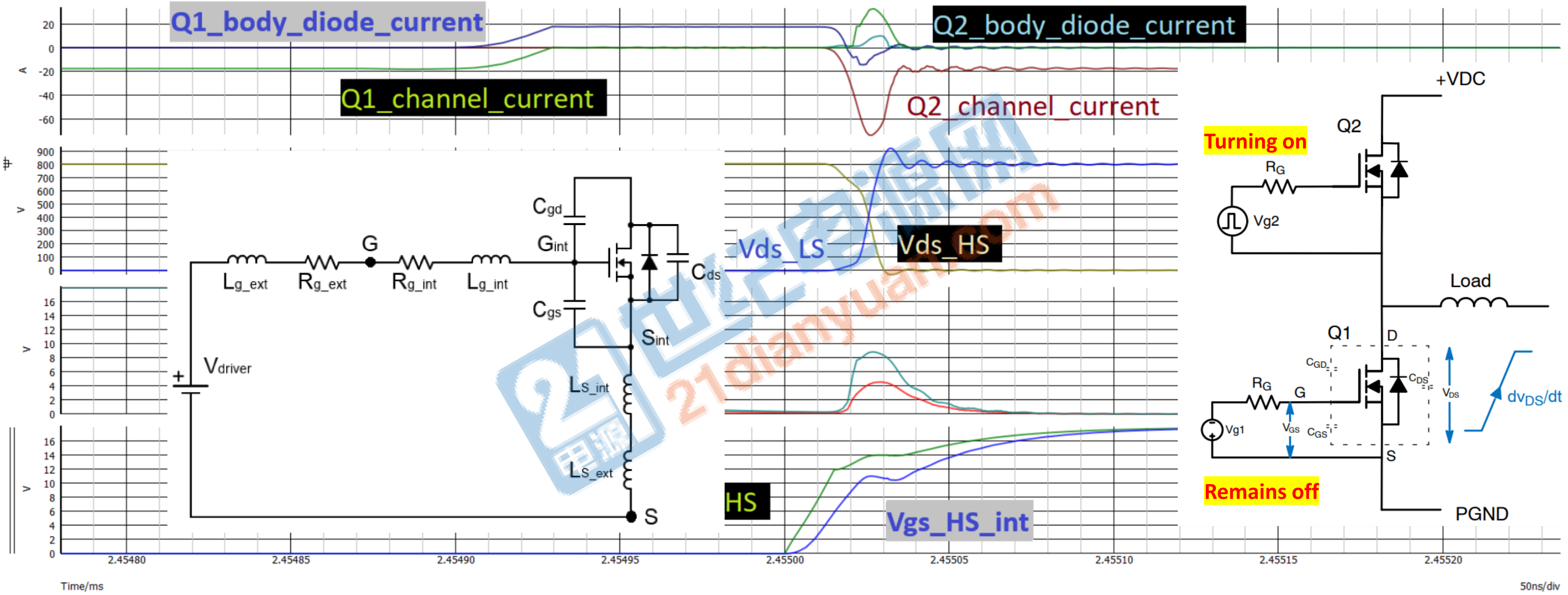
- Vgs→栅源极引脚电压；
- Vds→漏源极引脚电压；
- Vgs_int→晶圆内部栅源极电压；
- Channel Current→晶圆导通沟道电流；
- Body diode current→体二极管晶圆电流；

测试条件

- Vin = 800V;
- Rg = 4.7Ω ~ 25Ω;
- Vgs_on = +18V;
- Vgs_off = 0V, -3V;
- Load current = 20A ~ 40A;
- Duty cycle = 48.7%;
- Frequency = 100KHz;



半桥变换器低侧MOSFET的寄生导通问题 Rg ＝ 4.7Ω



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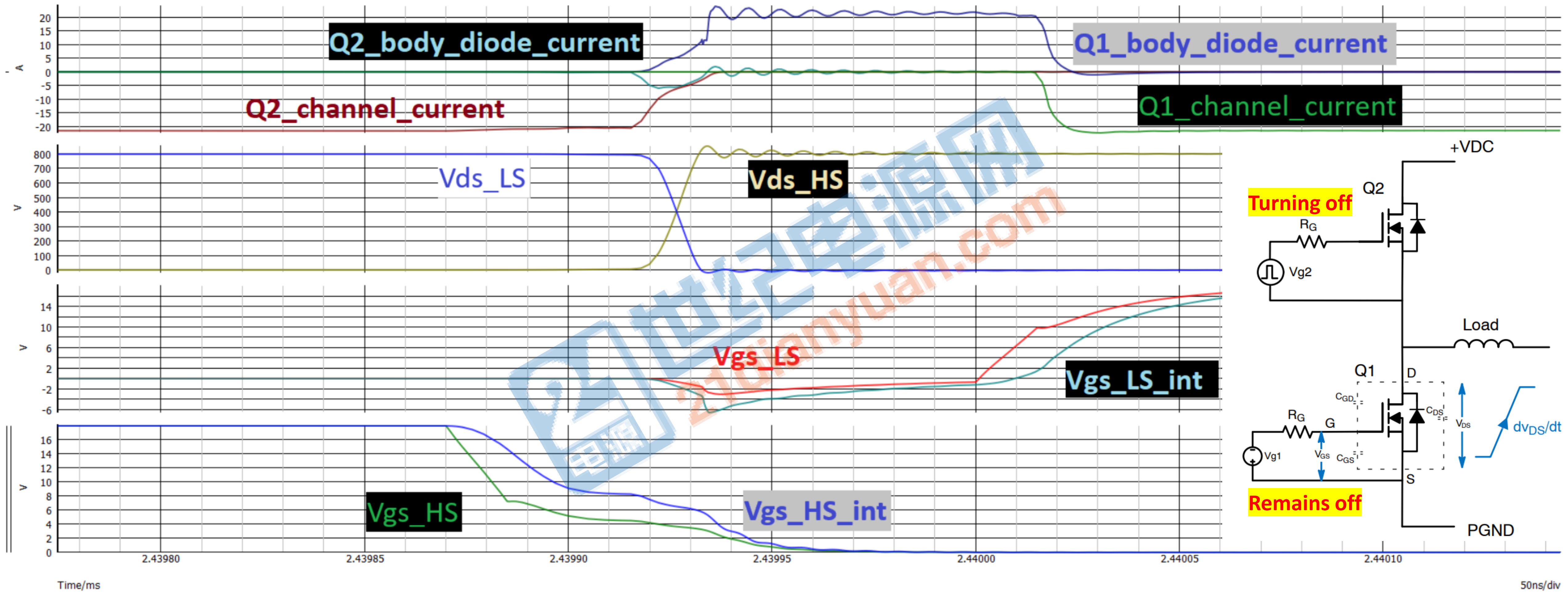
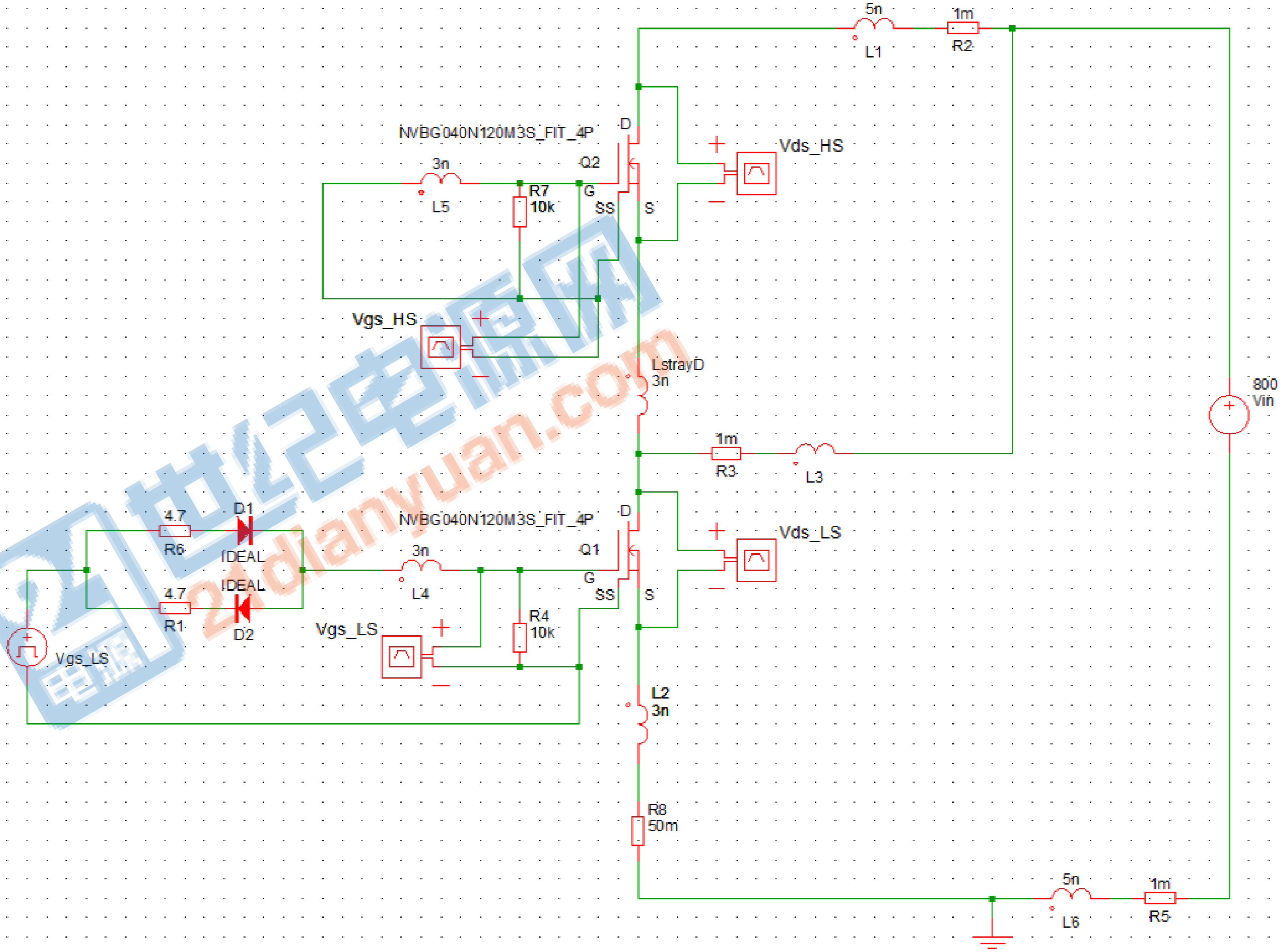
半桥变换器低侧MOSFET的寄生负压尖峰问题 Rg = 4.7Ω



双脉冲测试电路观察PTO寄生误导通现象

测试条件

- Vds = 800V；
- CH1：VGS_LS (6 V/div)；
- CH2：VDS_LS (300 V/div)；
- CH3：VSD_HS (300 V/div)；
- CH4：ID (20 A–40 A/div)；
- CH5：VGS_HS (6 V/div)；



开关波形Vgs_off = 0 V, ID = 40 A Rg_on/off = 4.7/4.7 Ω有无米勒钳位对比

Vds = 800V;

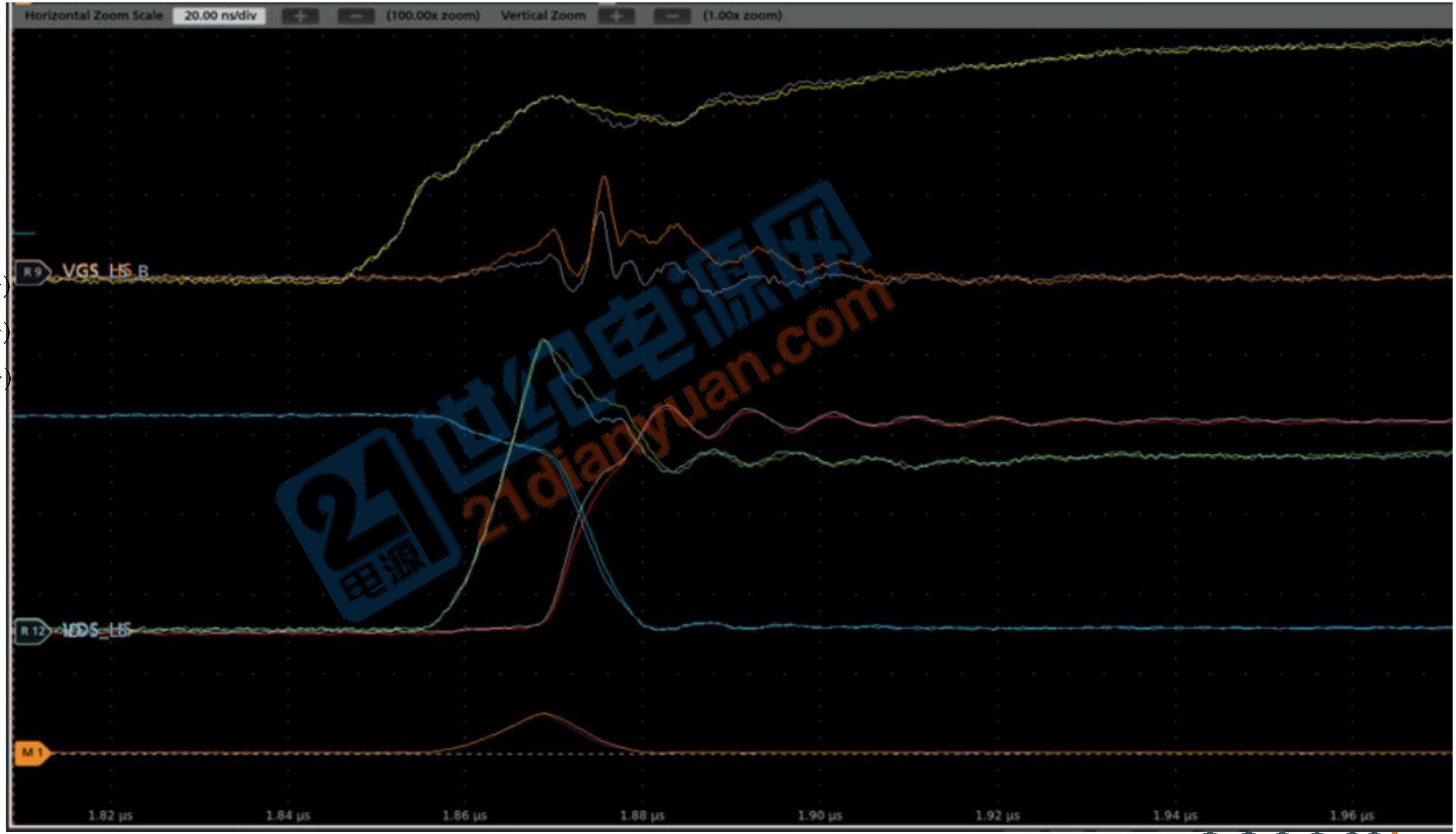
CH1: VGS_LS (6 V/div);

CH2: VDS_LS (300 V/div)

CH3: VSD_HS (300 V/div)

CH4: ID (20 A–40 A/div)

CH5: VGS_HS (6 V/div);



开关波形Vgs_off = 0 V/-3V, ID = 40 A Rg_on/off = 4.7/4.7 Ω无米勒钳位

Vds = 800V;

CH1: VGS_LS (6 V/div);

CH2: VDS_LS (300 V/div);

CH3: VSD_HS (300 V/div);

CH4: ID (20 A—40 A/div);

CH5: VGS_HS (6 V/div);

开关波形Vgs_off = 0 V/-3V, ID = 40 A Rg_on/off = 4.7/4.7 Ω有米勒钳位

Vds = 800V;

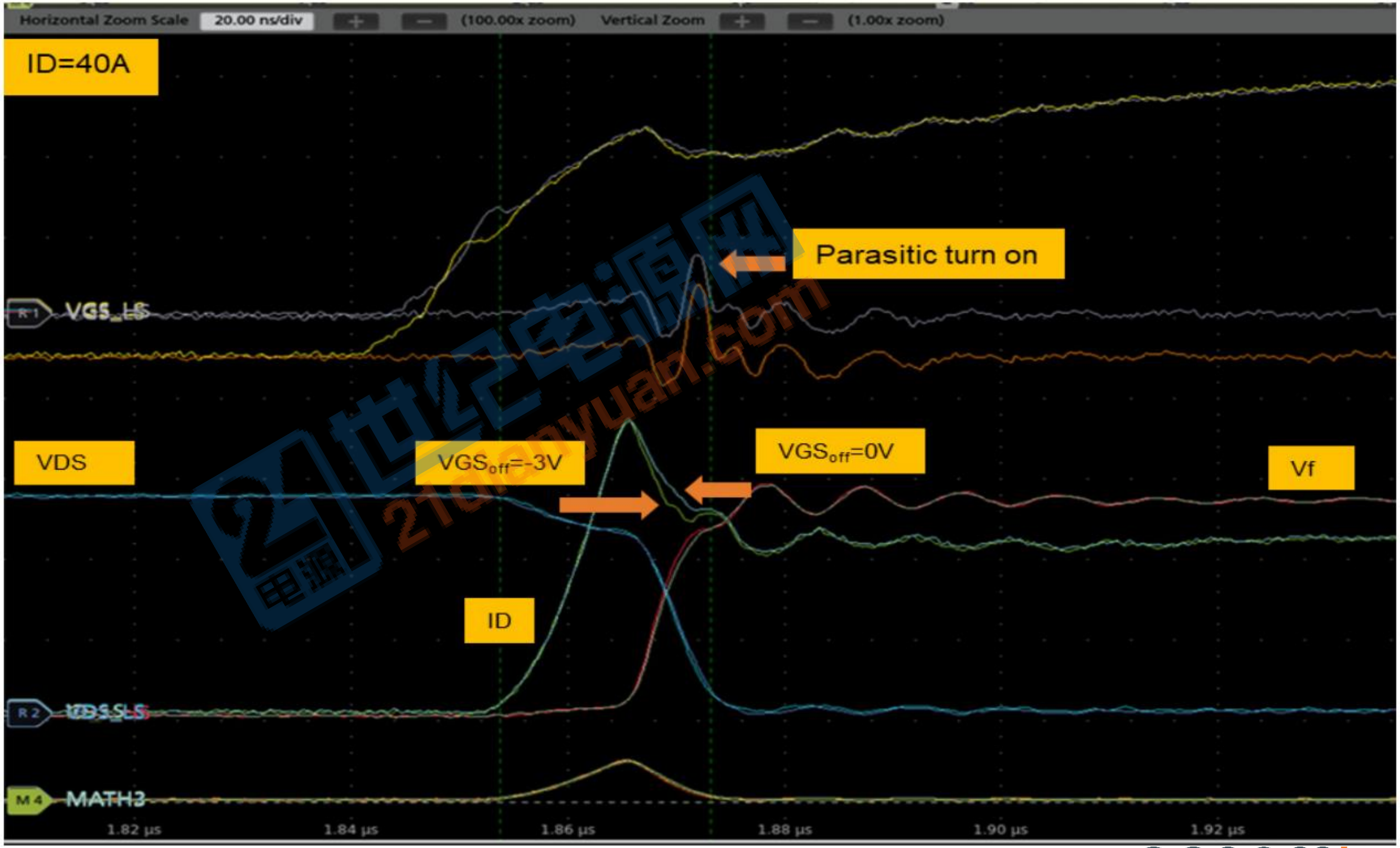
CH1: VGS_LS (6 V/div);

CH2: VDS_LS (300 V/div);

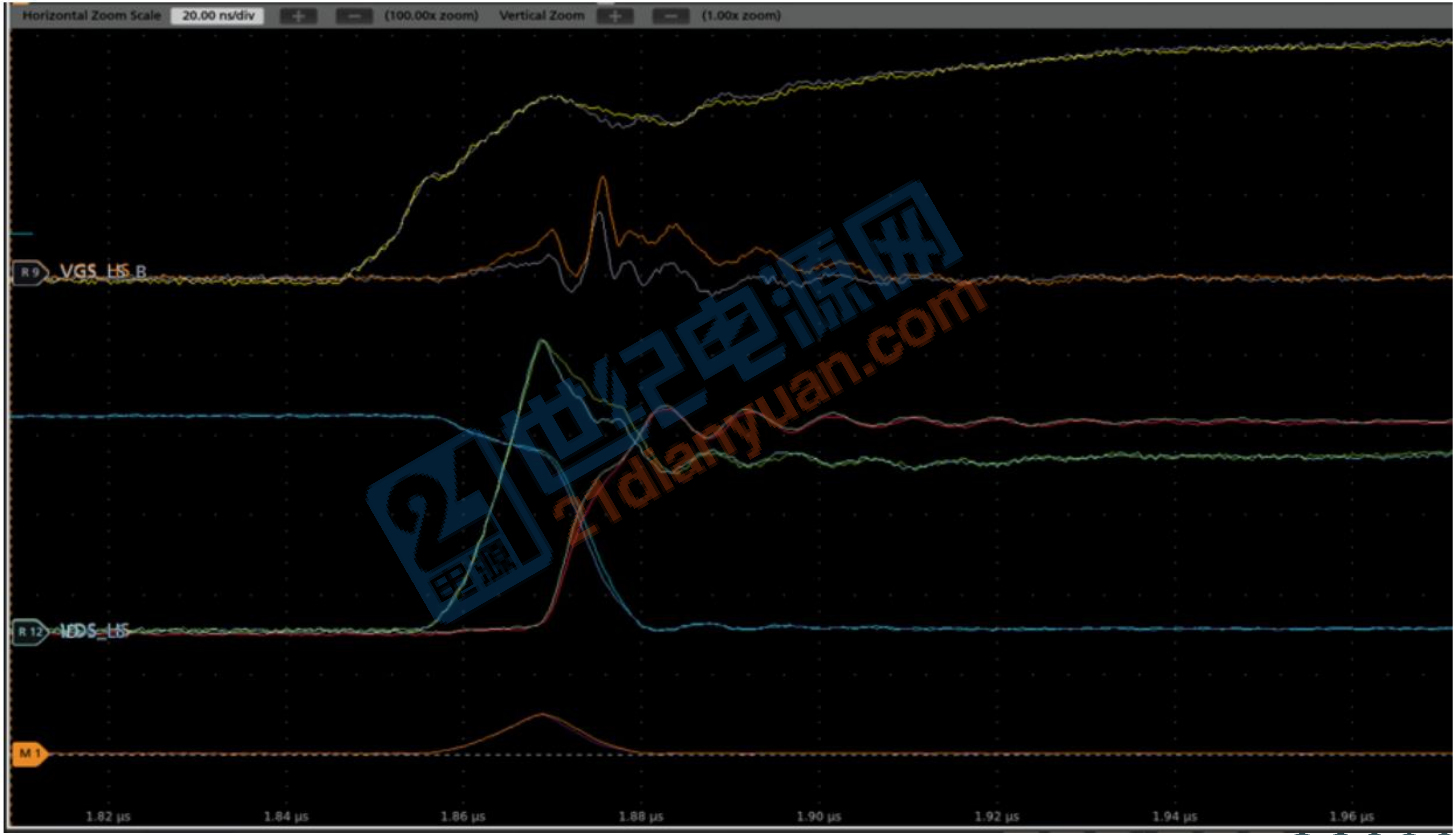
CH3: VSD_HS (300 V/div);

CH4: ID (20 A–40 A/div);

CH5: VGS_HS (6 V/div);



开关波形Vgs_off = 0 V, ID = 40 A Rg_on/off = 10/4.7 Ω无米勒钳位



I_D (A)	Rg_on (Ω)	Rg_off (Ω)	Vgs_off (V)	dv/dt Rising (V/ns)	dv/dt Falling (V/ns)	di/dt (A/ns)	Eon (μJ)	Eoff (μJ)
40	4.7	4.7	−3	129	103	7.137	444	146
40	4.7	4.7	0	120	95.74	7.133	456	182
40	10	4.7	−3	89.29	45.82	4.745	611	146
40	10	4.7	0	50	46	4.6	622	182

SiC VS. Si

- 增大Rg_on/Rg_off比值使用0V关断电压同样可以有效减小栅极串扰带来的误导通风险但是会增大开关损耗；
- 使用有米勒钳位功能的隔离驱动结合0V关断电压可以避免牺牲开关速度，而导致的较大开关损耗。

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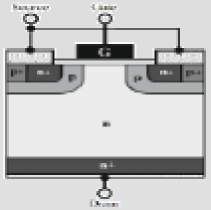
onsemi EliteSiC Leadership: From Substrate to Systems

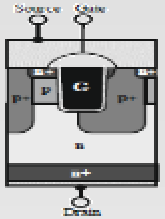
Substrates / Epi

- 150/200mm SiC wafering & epi fully internal in **onsemi** today

Fab



SiC Planar available today

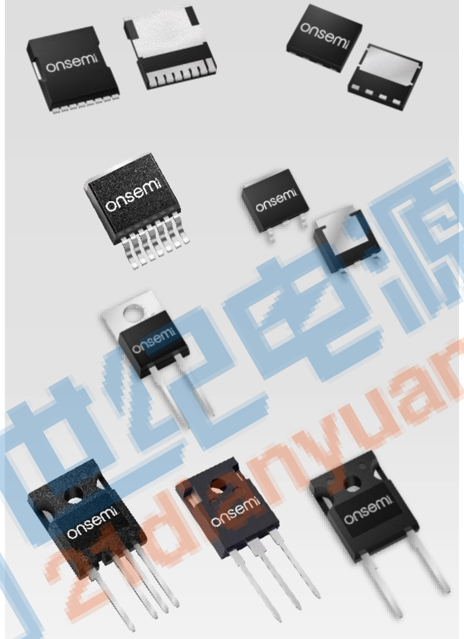


Working on trench for the future

200mm migration ready

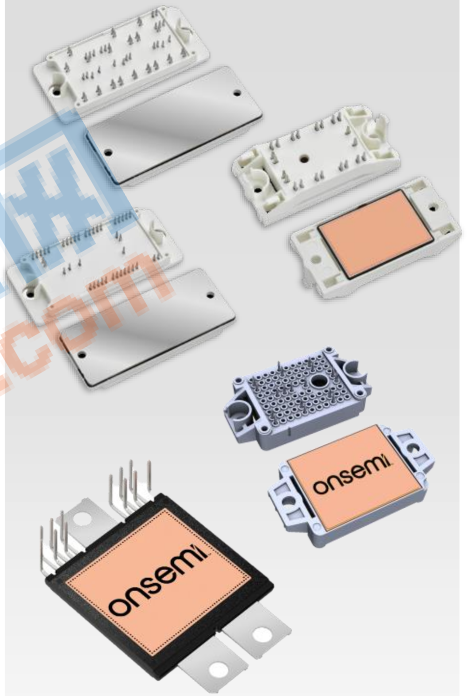
- Fabs ready today for 150mm→200mm migration

Devices / Die



- Full portfolio of diodes & MOSFETs
- Broad base of packages
- Die only & metal options
- Auto & Industrial devices

Modules



- Case & transfer molded options
- Full portfolio of hybrid & full SiC modules
- Single & dual cooling, direct & indirect

Systems

- Deep application & system know-how for automotive & industrial
- EMEA, US, Asia based apps support

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onsemi SiC MOSFET and Diode Families

Family	Series	Optimization	650V	900V	1200V	1700V	Primary Applications
M1	M1	Low RDS(ON) High SCWT			..120SC1	..170M1	Traction, On-board Charger, EV Charging Station, Solar, UPS/Energy Storage, High Power Industrial
M2	M2	Low RDS(ON) High SCWT	..065SC1	..090SC1			Traction, On-board Charger, EV Charging Station, Solar
M3	M3S	High speed	..065M3S		..120M3S		On-board Charger, EV Charging Station, Solar
	M3P, M3e	Low RDS(ON) High SCWT			..120M3x SCWT dependent		Traction, UPS/Energy Storage, High Power Industrial

Family	Optimization	650V		1200V	1700V	Primary Applications
D1	High IFSM	..065A		..120A	..170A	On-board Charger, EV Charging Station, Solar, UPS/Energy Storage, High Power Industrial
D2	Low QC	..065B				On-board Charger, EV Charging Station, Solar
D3	Low QC x VF			..120C		On-board Charger, EV Charging Station, Solar, UPS/Energy Storage, High Power Industrial

Traction On-board Charger EV Charging Station UPS/Energy Storage Solar High Power Industrial

In Development

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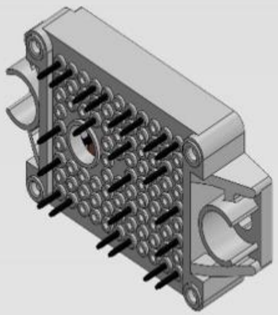
Gel-filled Modules for Energy Infrastructure

F1



1.2 mm press-fit pins
Solder pins

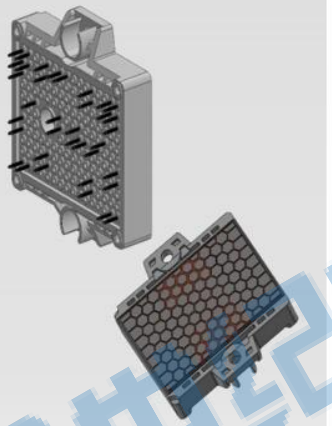
With TIM/no TIM

Q0

1.2 mm press-fit pins
1.6 mm press-fit pins
Solder pins

With TIM/no TIM

F2



1.2 mm press-fit pins
Solder pins

With TIM/no TIM

Q1

1.2 mm press-fit pins
1.6mm press-fit pins
Solder pins

With TIM/no TIM

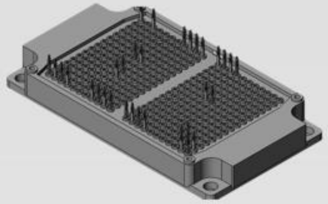
Q2

with base plate

1.6 mm press-fit pins
Solder pins

With TIM/no TIM

F5+BP

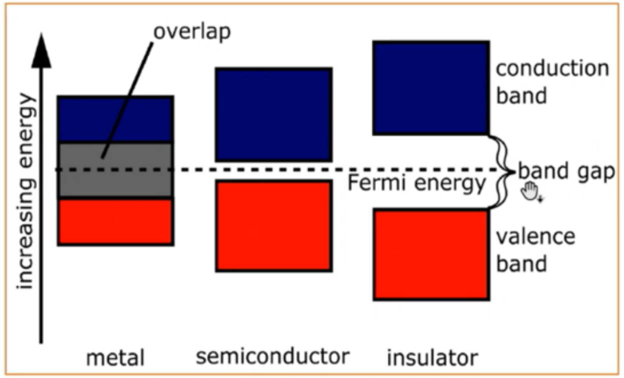


with base plate

1.2 mm press-fit pins
Solder pins

With TIM/no TIM

Key Takeaway！



"A comparison of the band gaps of metals, insulators and semiconductors," by inductiveload CC A-SA 2.5

宽禁带：Eg＞2.3 eV

- 宽禁带半导体定义：带隙能量 Eg＞2.3eV ；
- 在光伏逆变应用中使用碳化硅方案代替IGBT可以实现更低的BOM成本；
- on
- 软
- 存
- 的

度

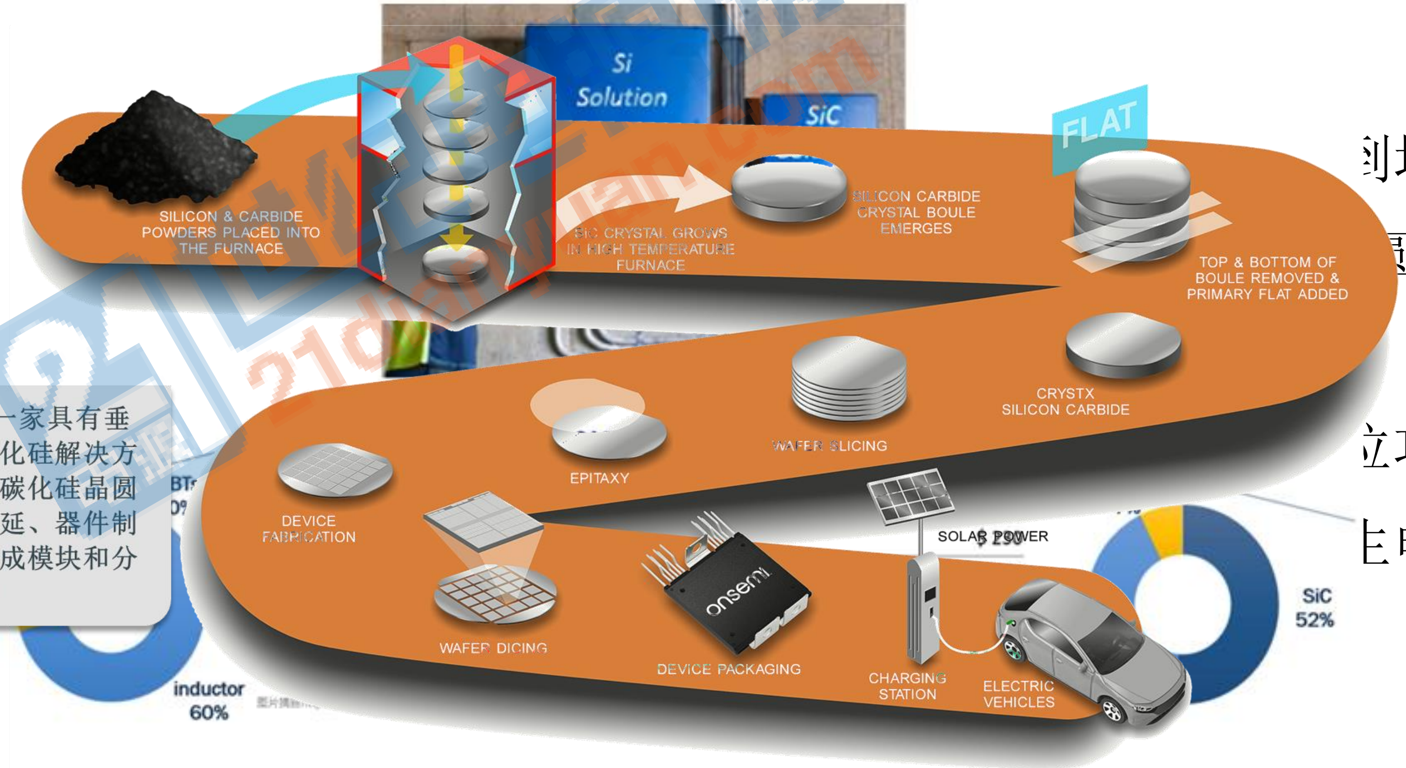
米

到均流目

固具有高

立功能的

E电容带



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