基于网分的TDR测试测量技术

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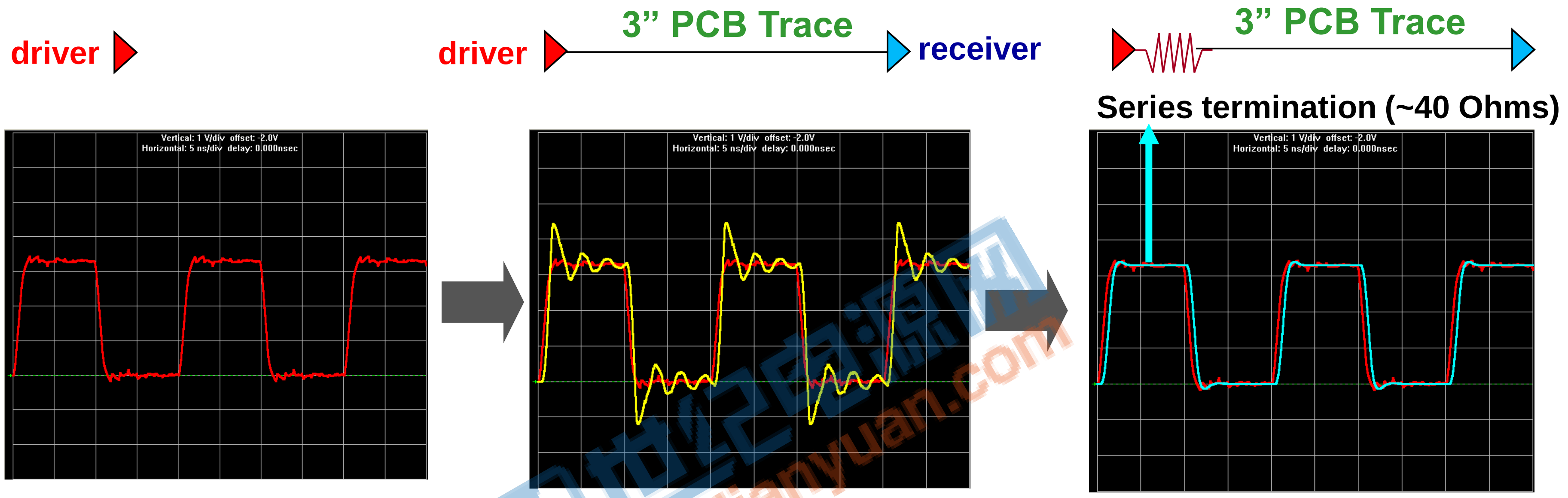
KEYSIGHT TECHNOLOGIES

What Is Signal Integrity?



Signal Integrity = Where the electrical properties of the interconnects can cause significant distortions in digital signals.

- >1 GHz of bandwidth
- <1 ns risetime
- Typically >2 Gb/s data rate with embedded clock

Signal Integrity = Paying attention to RF effects, ie. impedance

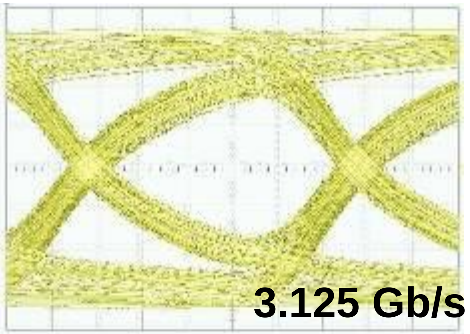
The Reality Is That FR4 Limits Your Options

–FR4 is common, low cost and easy to manufacture

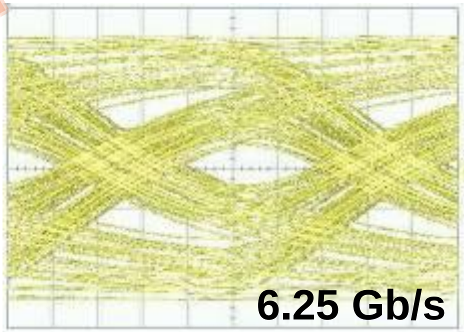
–BUT it has problems:

- Reflections at high speeds
- Dispersion varies with frequency
- High Insertion Loss
- ISI induced Jitter
- Effects vary with temperature and humidity

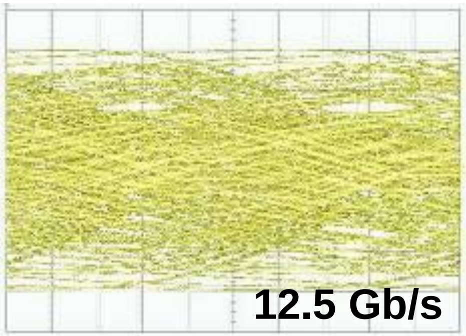
What Works Today



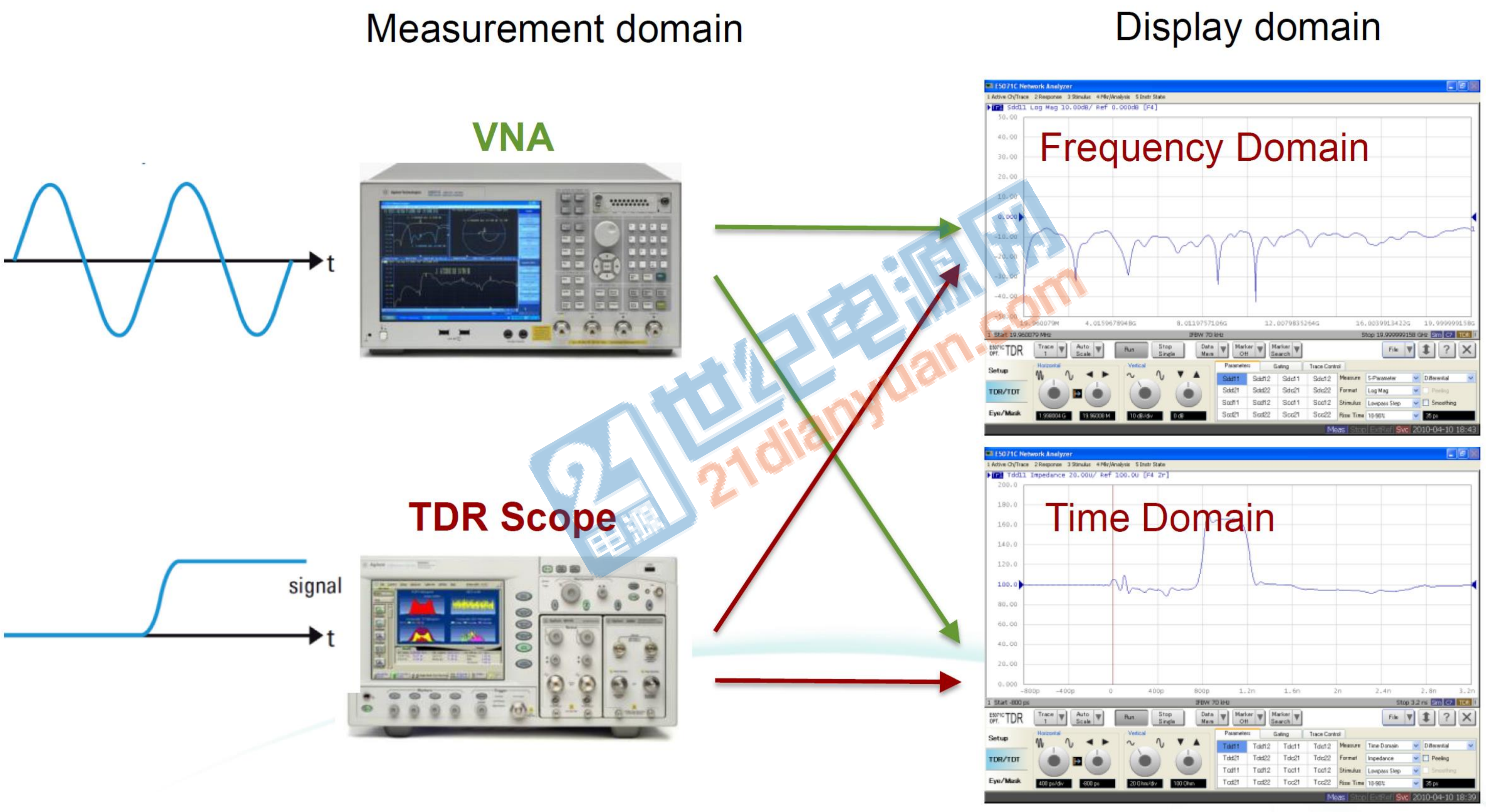
Gets Worse The Next Time



Then Stops

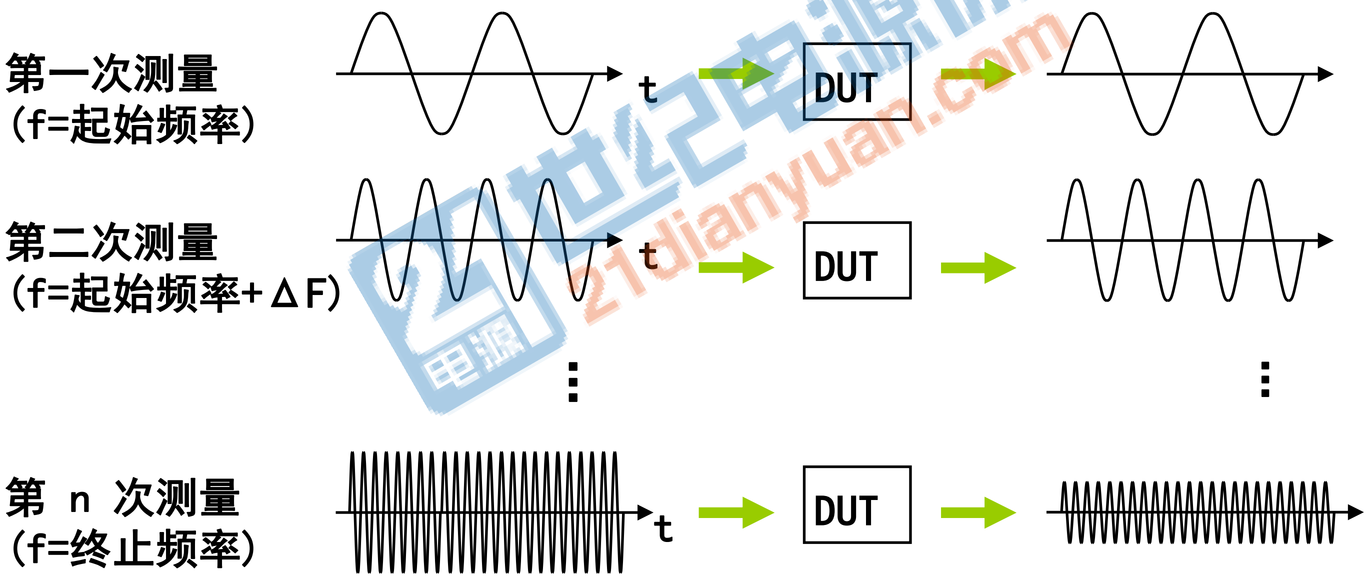


基于网分TDR vs 基于采样示波器的TDR



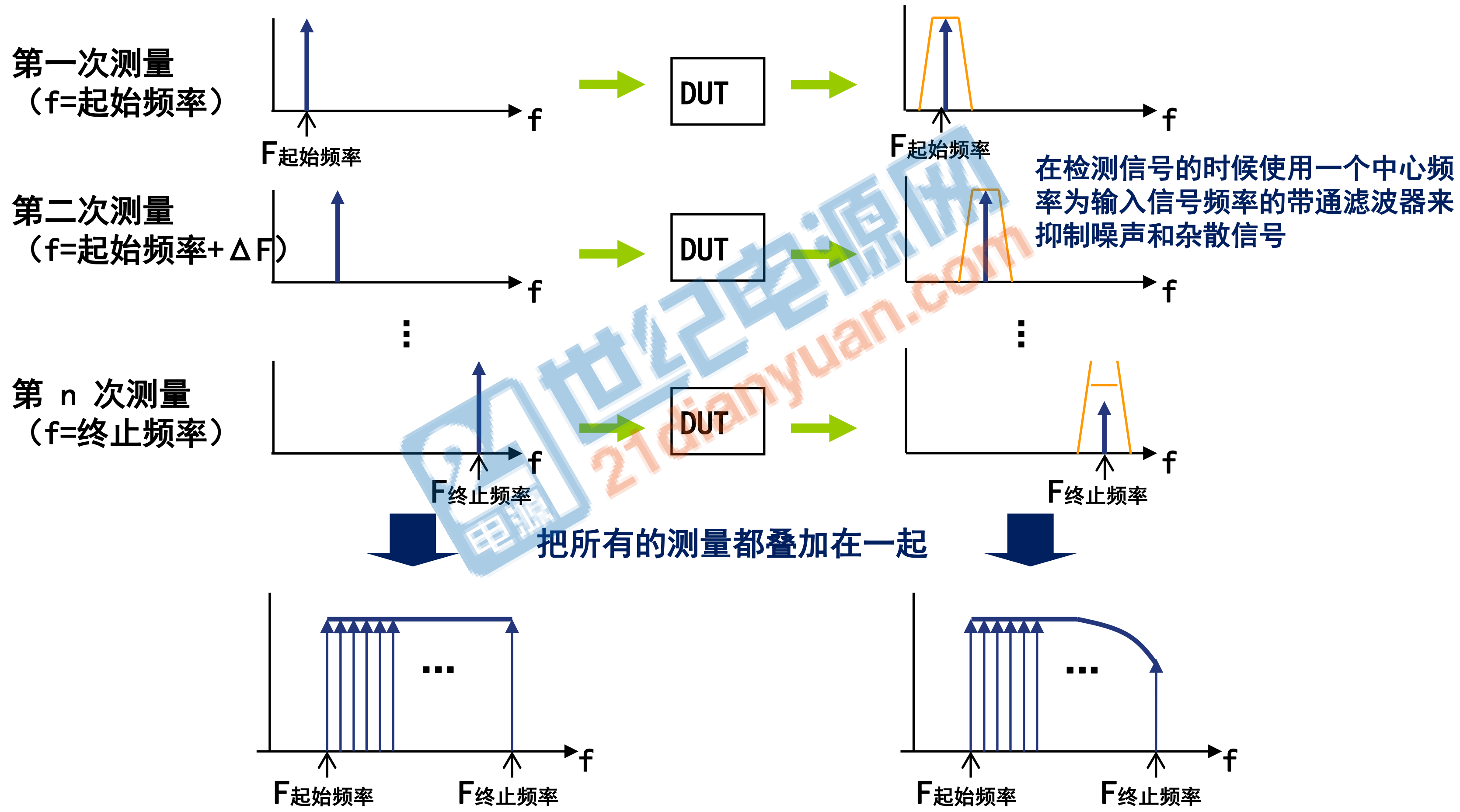
矢量网络分析仪进行测量的过程

在不同的频率点上反复重复同样的测试，测试频率逐渐提高（频率扫描）



矢量网络分析仪在频率域内进行测量

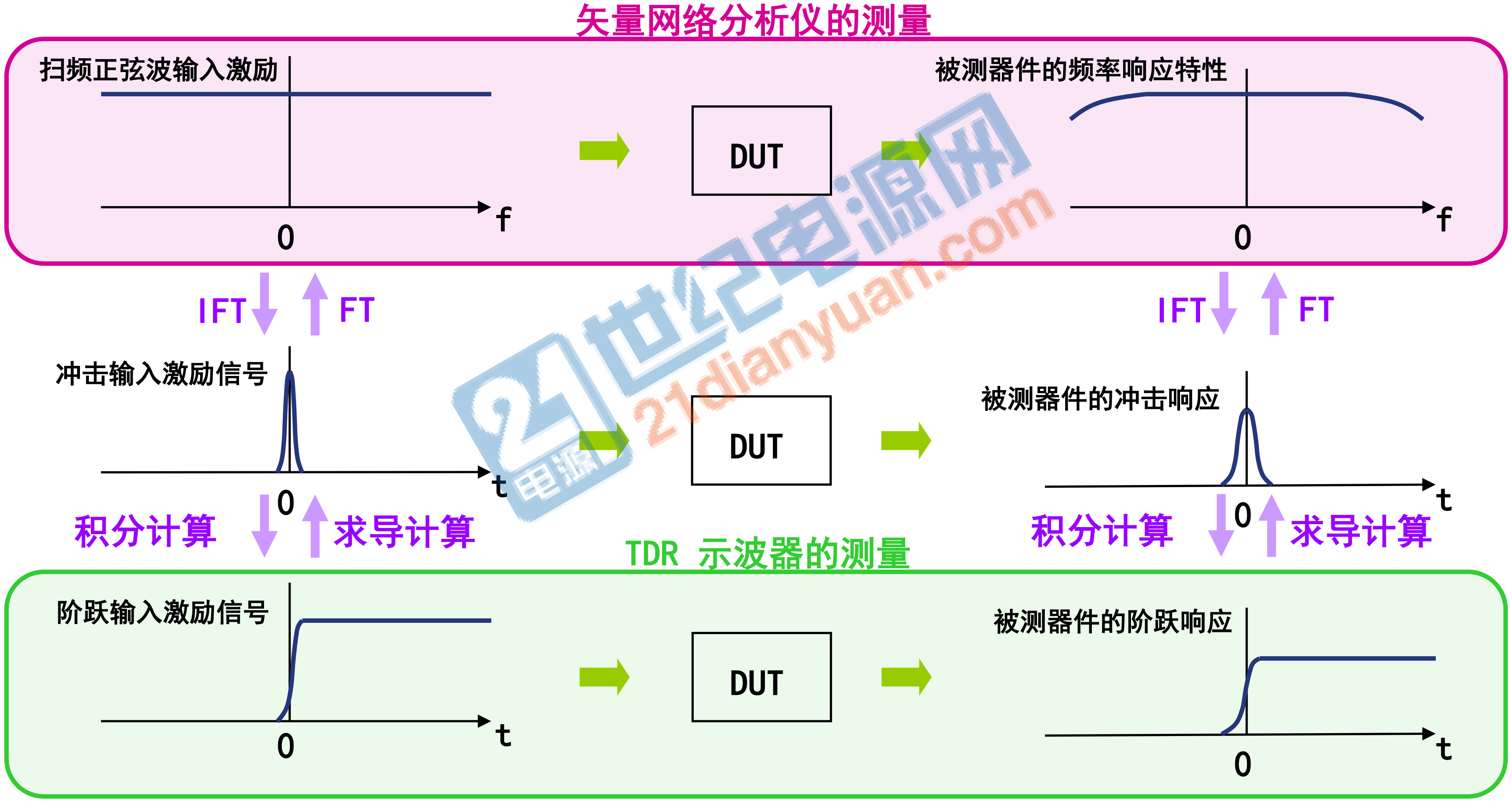
在不同的频率点上反复重复同样的测试，测试频率逐渐提高（频率扫描）



怎样能把器件的频率响应特性转化为时域的冲击响应特性和阶跃响应特性？

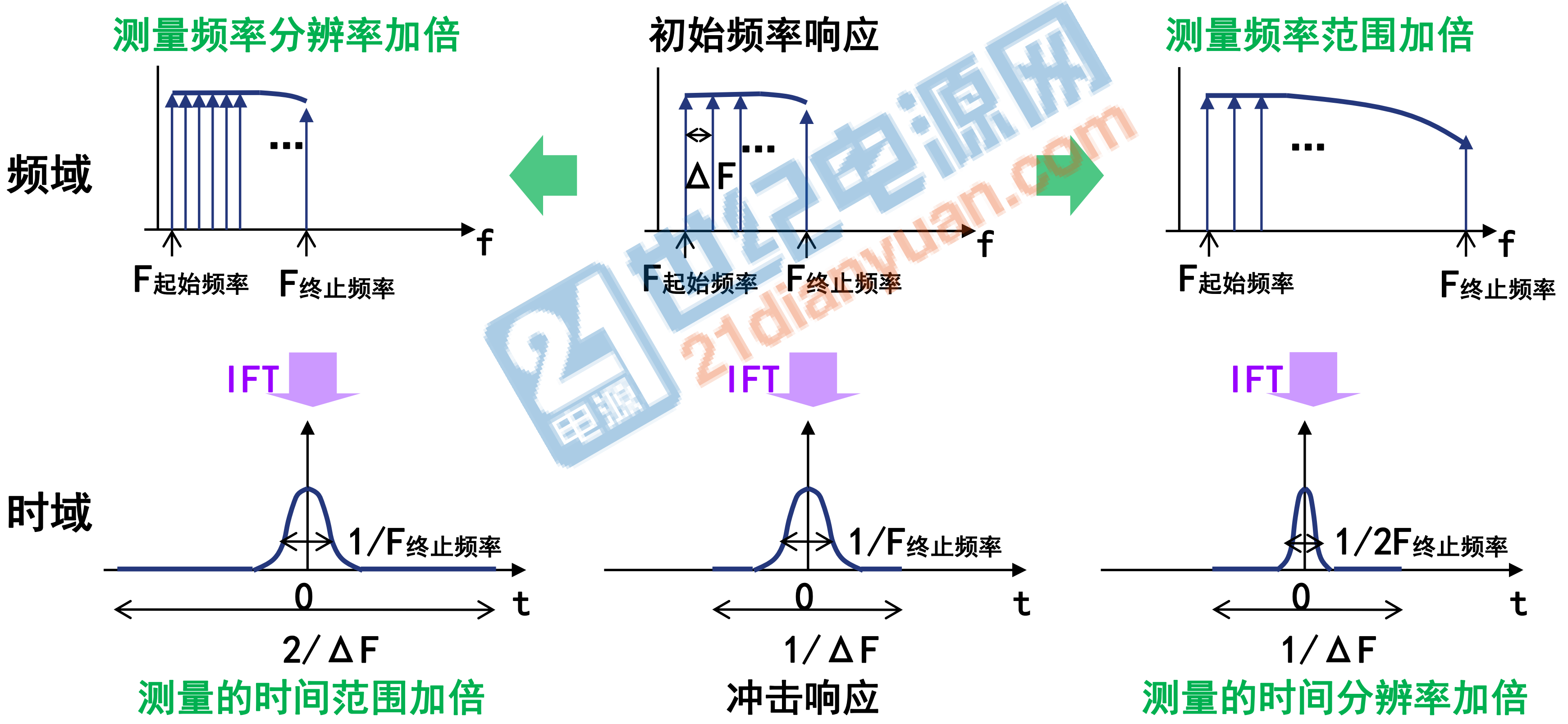
怎样把频域响应转化为时域响应

冲击响应可以使用反傅立叶变换计算出来
通过积分计算可以把冲击响应变换成阶跃响应



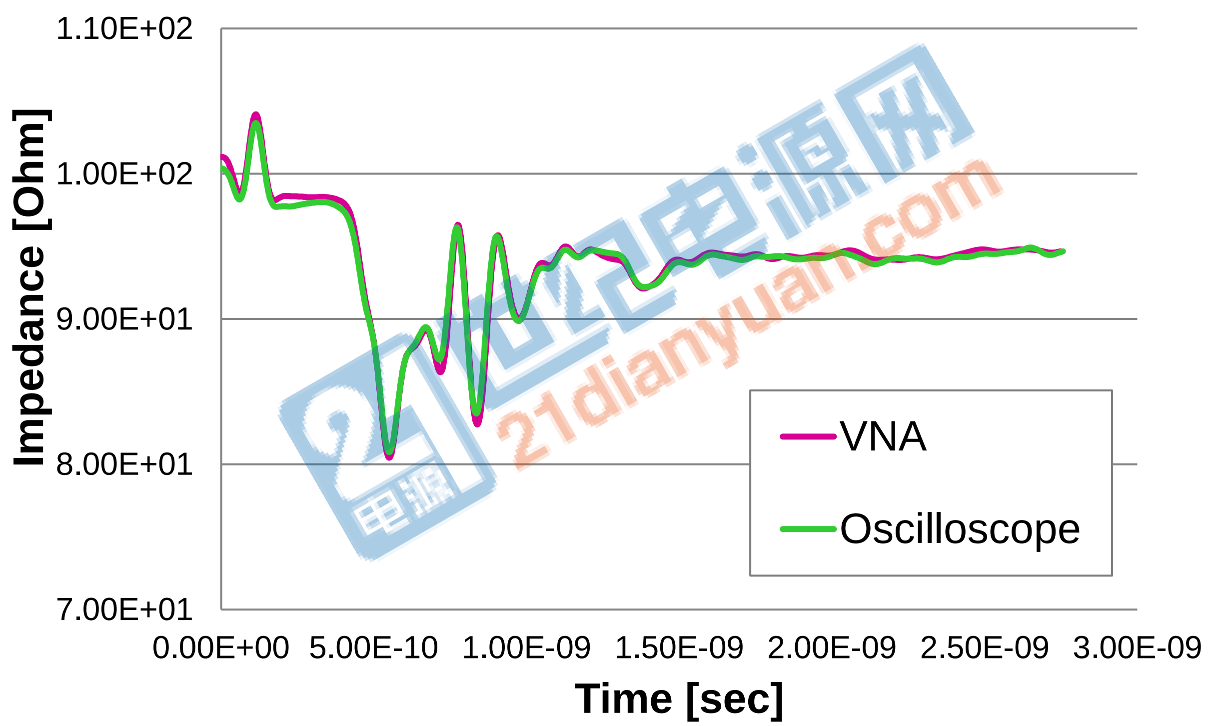
时域和频域的关系

如果测量频率的分辨率提高一倍，则测量的时间范围也增加一倍
如果测量的频率范围增加一倍，则测量的时间分辨率也提高一倍



TDR 示波器测量结果和矢量网络分析仪测量结果的比较

使用 TDR 示波器和矢量网络分析仪对 USB 3.0 测试夹具进行阶跃响应测试结果的比较

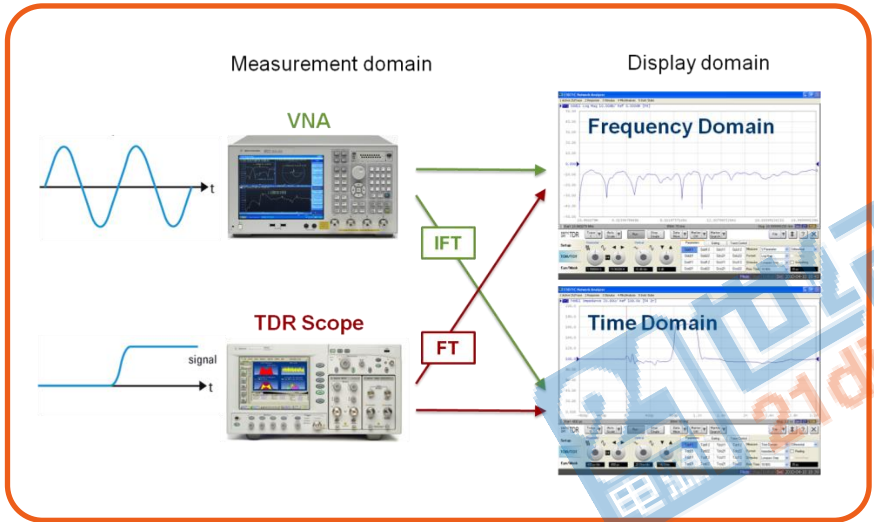


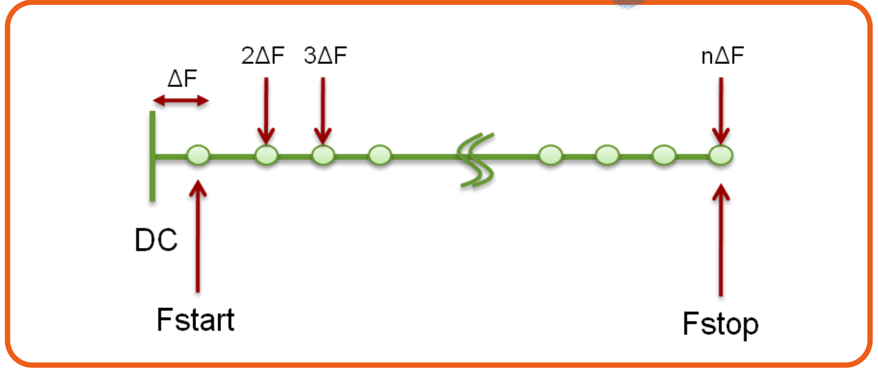
TDR 示波器的测试结果和矢量网络分析仪的测试结果相差只有 0.4 Ω_{RMS} 测试结果非常一致！

传统的网分时域应用在TDR的限制

Page

Modern Vector Network Analyzers (VNAs) have the capability to display the time domain response by using Fourier theory. Although the VNA provides a TDR-like display, there are differences between the traditional TDR and VNA time domain techniques.





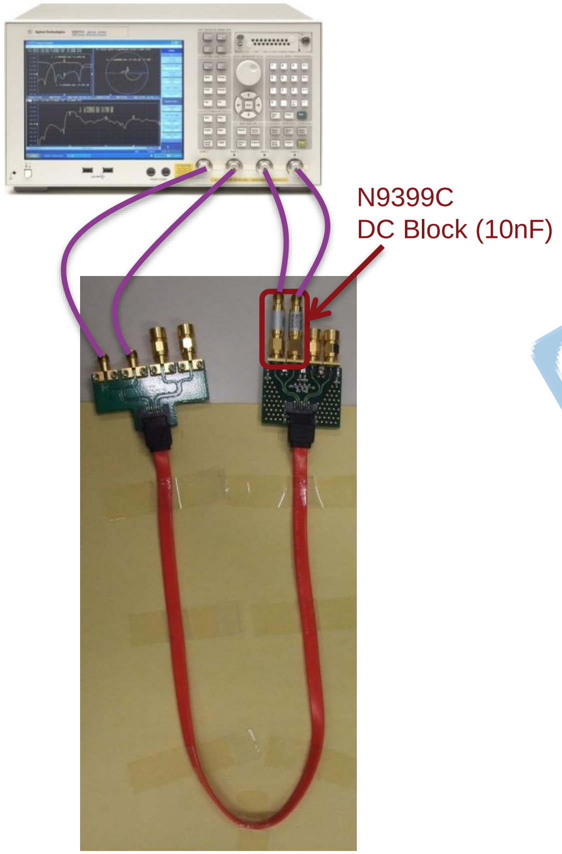
One key difference is the lower frequency limit of the VNA.

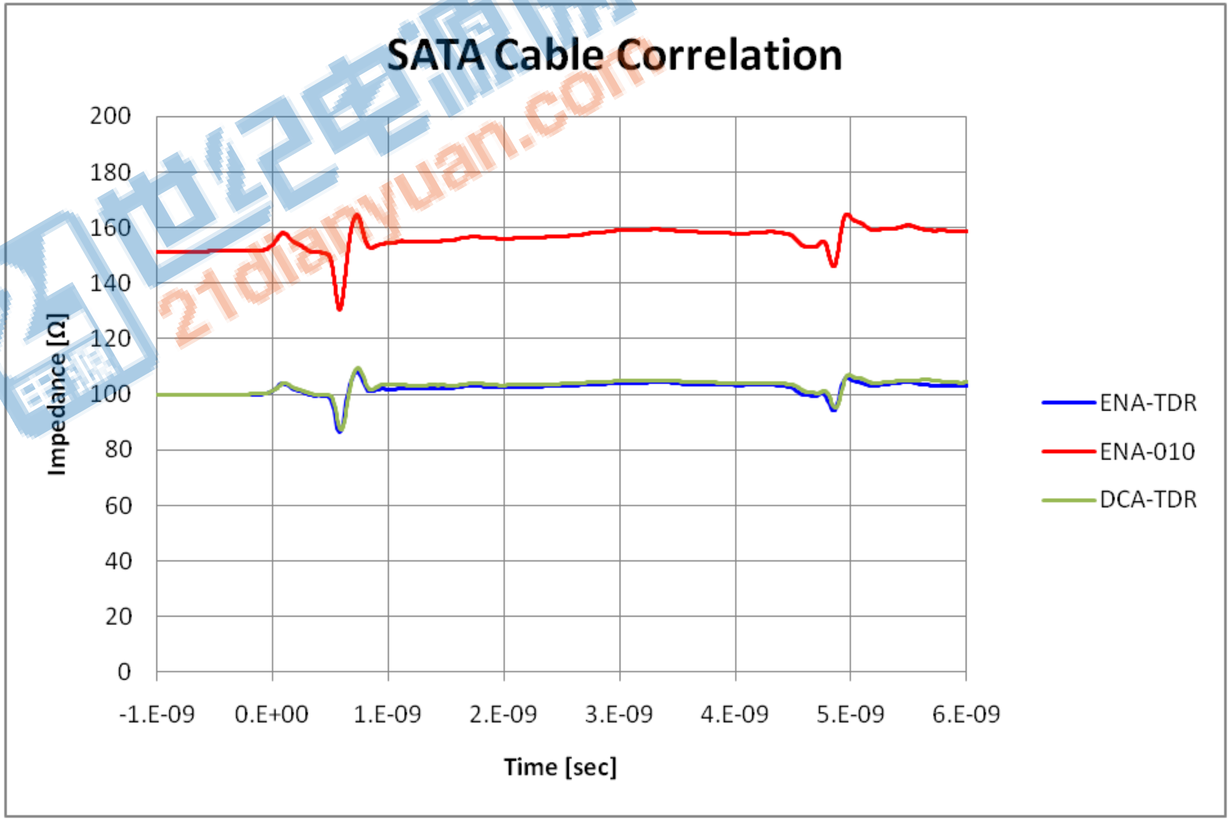
The Fourier Transform includes the effects of the DC value on the frequency response. The DC value is required to generate the step stimulus.

Since the VNA does not measure the DC response, the DC value must be extrapolated. In the case of **ENA Option 010**, the DC term is extrapolated from the first few data points in the frequency domain. This extrapolation method is sufficient in most cases, but significant errors are introduced when measuring devices with long transient response, such as AC coupled circuits.
With **ENA Option TDR**, a new algorithm is implemented to estimate the DC response which allows for accurate results even when measuring devices with long transient response, such as AC coupled circuits.

传统的网分时域应用在TDR的限制

ENA Option TDR is more accurate than Traditional VNA-based Time Domain measurements

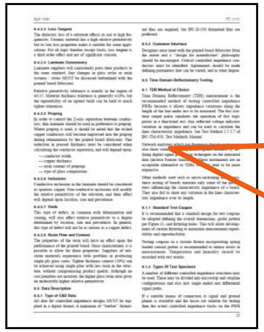




IPC Standard

ENA Option TDR as Standard Measurement Solution for PCB

IPC-2141 Controlled Impedance Circuit Boards and High Speed Design



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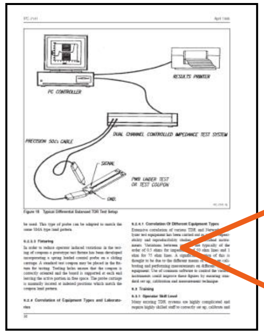
9.1 TDR Method of Choice

Network analyzers which use frequency domain testing can also show variations of impedance against distance by utilizing digital signal processing techniques on the measured data (inverse Fourier transform). These instruments are an acceptable alternative to TDRs but they tend to be more expensive.



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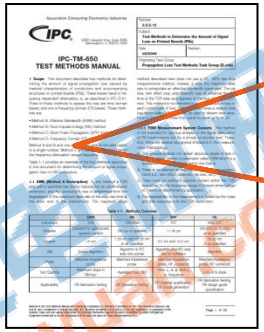
9.2.4.1 Correlation Of Different Equipment Types

Extensive correlation of various TDR and Network Analyzer test equipment has been carried out as well as repeatability and reproducibility studies on individual instruments. Variations between systems are typically of the order of 0.5 ohms for impedances of 50 ohm lines and 1 ohm for 75 ohm lines. A significant portion of this is thought to be due to the different means of setting up calibrating and performing measurements on different types of equipment. Use of common software to control the various instruments could improve these figures by ensuring standard set up, calibration and measurement technique.

Source:
http://kazus.ru/nuke/modules/Downloads/pub/147/0/IPC%202141%20Controlled%20Z%20PCB%20.pdf

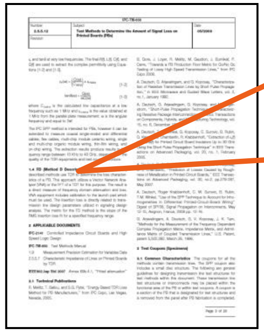
IPC-TM-650 Number 2.5.5.12 Test Methods to Determine the Amount of Signal Loss on Printed Boards (PBs)



Page 1

1 Scope This document describes four methods for determining the amount of signal propagation loss caused by material characteristics of conductors and accompanying structures on printed boards (PBs). These losses result in frequency dependent attenuation, α, as described in IPC-2141. Three of these methods to assess this loss are time domain based, and one is frequency domain (FD) based. These methods are:

- Method A: Effective Bandwidth (EBW) method
- Method B: Root Impulse Energy (RIE) method
- Method C: Short Pulse Propagation (SPP) method
- Method D: Frequency Domain (FD) method



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1.4 FD (Method D Description) Two of the previously described methods use TDR to determine the loss characteristics of a PB. This approach utilizes a Vector Network Analyzer (VNA) or the FFT of a TDT for this purpose. The result is a direct measure of frequency domain attenuation and loss. VNA equipment includes calibration to the launch pad which must be used. The insertion loss is directly related to transmission line design parameters utilized in signaling design analysis. The metric for the FD method is the slope of the RMS insertion loss fit for a specified frequency range.

Source:
http://www.ipc.org/4.0_Knowledge/4.1_Standards/test/2-5_2-5-5-12.pdf

KEYSIGHT TECHNOLOGIES

阻抗测试设备关键指标

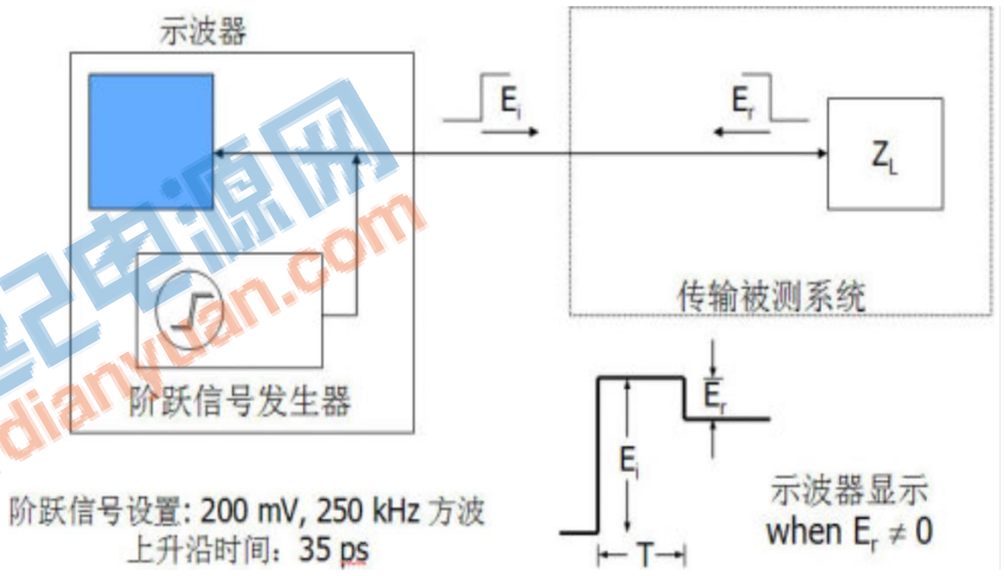
阶跃信号上升时间

最短可测距离/分辨率

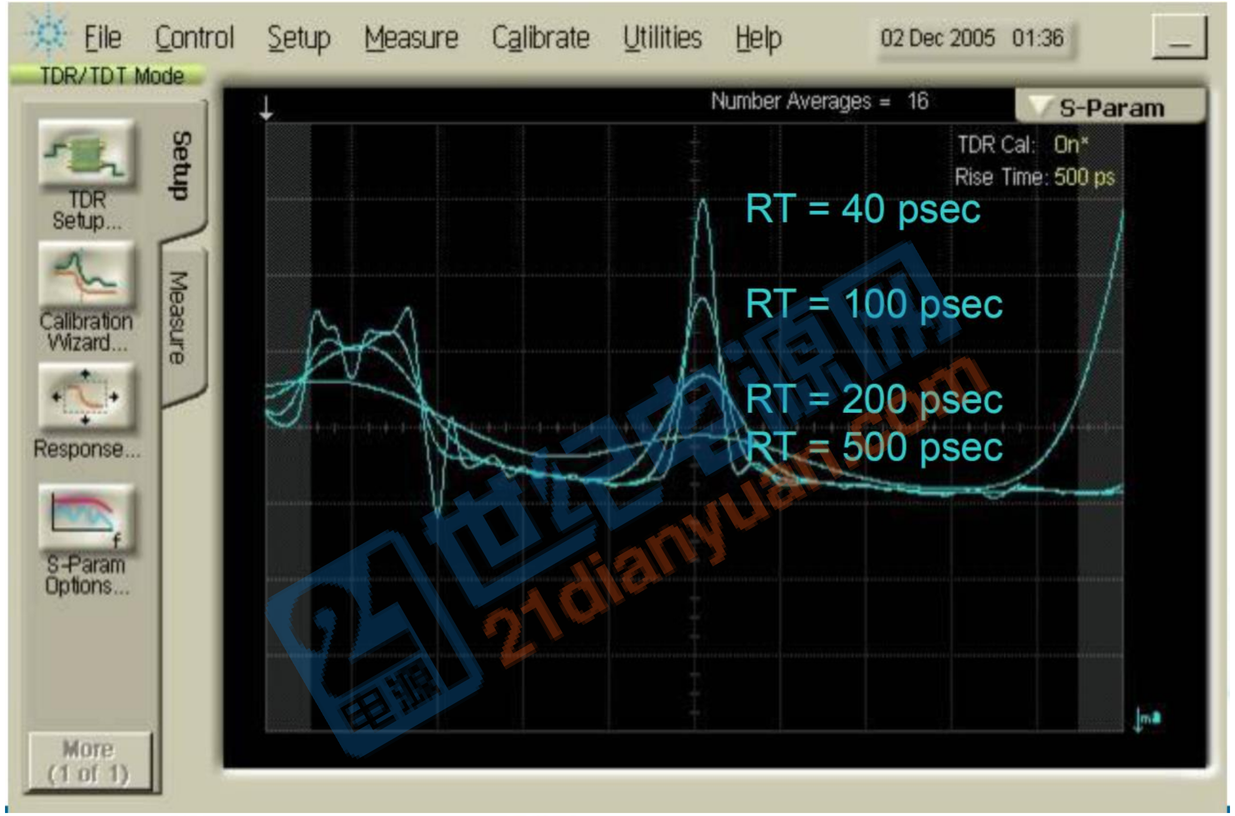
系统带宽 （主机+ 探头+ 射频线缆）

校准技术

屏蔽与静电防护



上升时间（RT Rise Time）vs 分辨率



上升时间越快，对阻抗不连续性的分辨率越高，

E5063A 上升时间 与相应分辨率

		E5063A	18GHz	8.5GHz	4.5GHz
Rise Time (LP Step)	Spec.	min (10-90%)	24.8 ps	52.4 ps	99.1 ps
Response Resolution	Typ.	min @ LP Step mode, reflection meas, in air (εr = 1)	3.72 mm	7.9 mm	14.9 mm
	Typ.	min @ LP Step mode, reflection meas, in FR4 (εr = 4.9)	**1.67 mm**	3.5 mm	**6.7 mm**

阻抗测试设备关键指标

阶跃信号上升时间

最短可测距离/分辨率

系统带宽 （主机+ 探头+ 射频线缆）

校准技术

屏蔽与静电防护

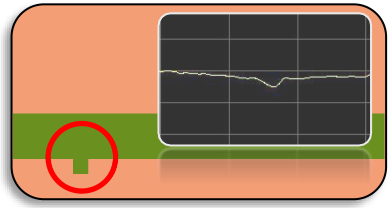
（是德网分抗3000V静电！！
节省静电/屏蔽房投入及后续维修费用）

Three Breakthroughs

for PCB Production and Quality Control

TDR & S Parameter

Fast & Accurate

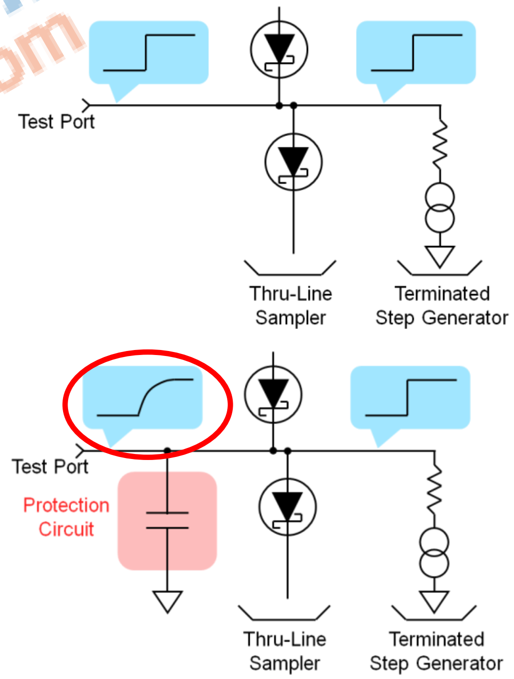


ESD Robustness

ESD Robustness

TDR Oscilloscopes

Implementing a protection circuit is difficult, because it will slow down the rise time of the step stimulus.

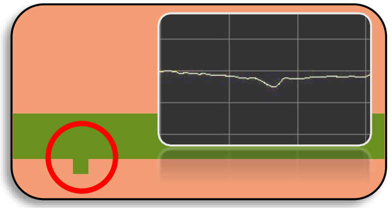


Three Breakthroughs

for PCB Production and Quality Control

TDR & S Parameter

Fast & Accurate

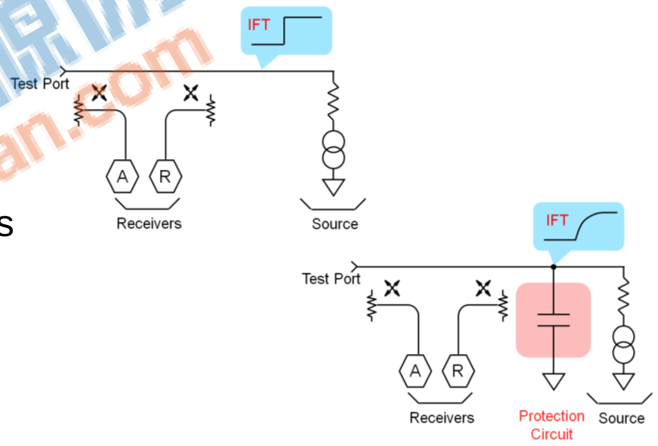


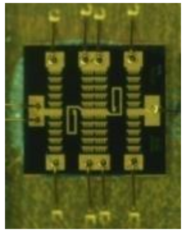
ESD Robustness

ESD Robustness

ENA Option TDR

VNA measures the vector ratios of the transmitted and received signals. Therefore, the effects of the protection circuit will be canceled out.





Proprietary ESD protection chip significantly increase ESD robustness, while at the same time maintaining **excellent RF performance** (22ps rise time for 20GHz models).

KEYSIGHT TECHNOLOGIES

Keysight 网分TDR阻抗特点

1.抗静电ESD(DC 3,000V)

2.一机多能，可进行

-TDR（单端，差分）**阻抗**，**损耗**测试

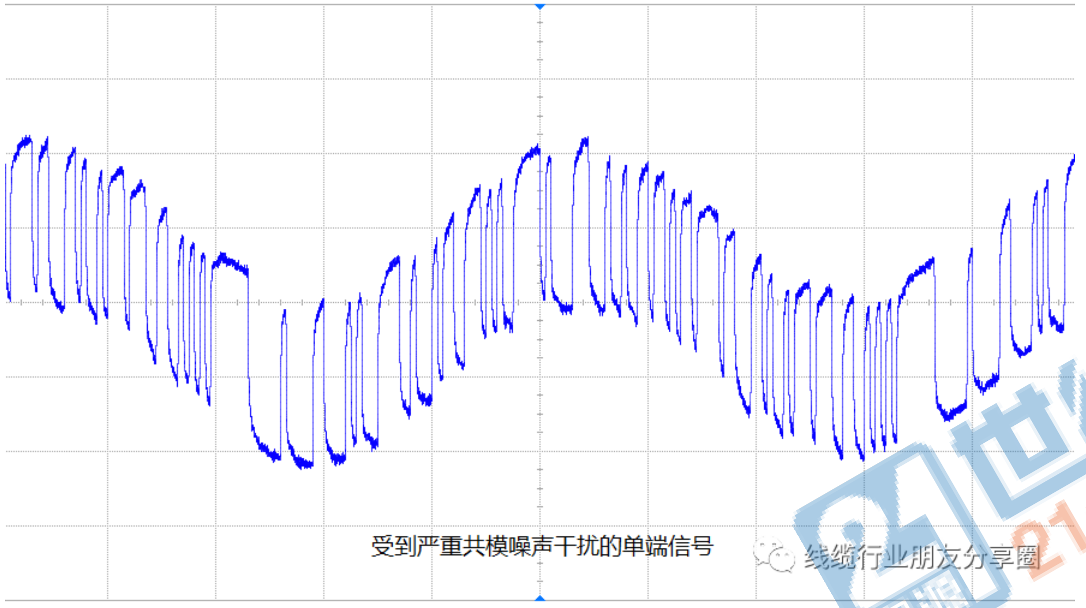
-板载天线**回波损耗**测试(Embedded Antenna Return Loss)，

-板材材料特性（如**介电常数Dk/损耗Df**）测试，需要材料测试软件N1500A +N1501AExx谐振腔。

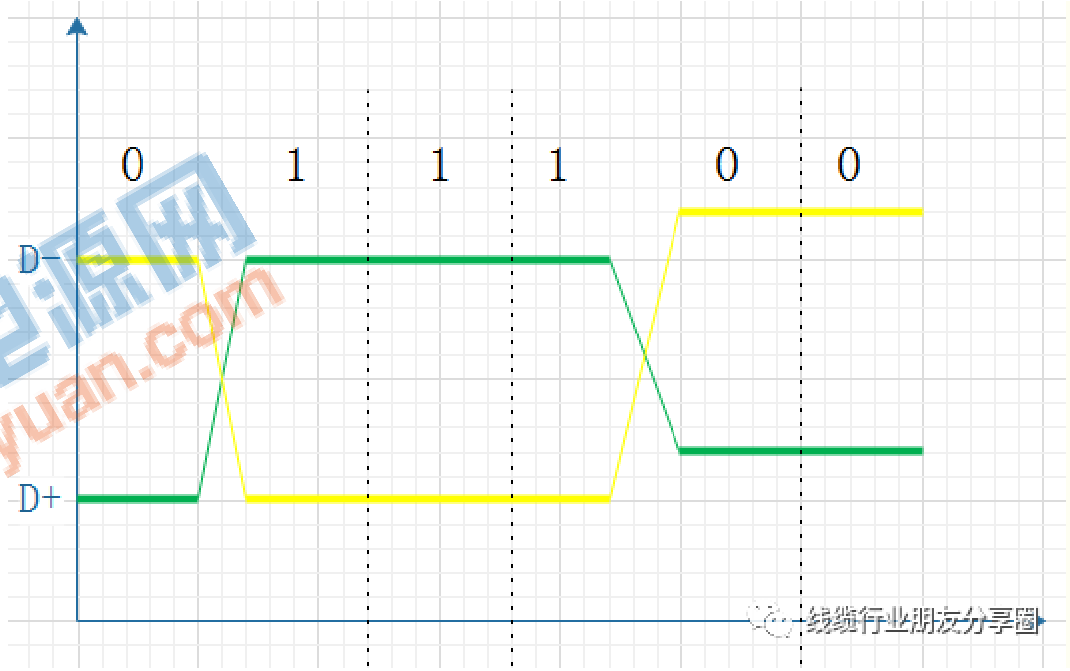
-Hot（有源带载）TDR（比如PC主板HDMI，USB端口）测试

3.高精度Accuracy (0.8Ω)，重复性 Repeatability(0.05Ω)

单端（不平衡）信号和差分（平衡）信号



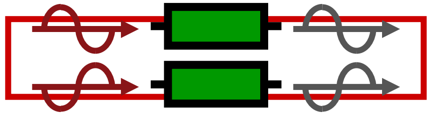
受到严重共模噪声干扰的单端信号



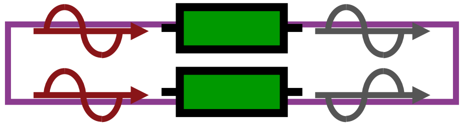
比较这两个电压的差值来判断发送端发送的逻辑状态

混合S参数反映平衡器件性能

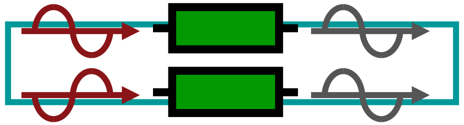
差分输入，差分响应
反映器件差分处理性能



共模输入，差分响应
模式转换指标
反映器件抗扰度性能

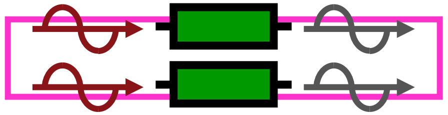


		差分激励 Port 1	差分激励 Port 2	共模激励 Port 1	共模激励 Port 2
差分响应	Port 1	S_{DD11}	S_{DD12}	S_{DC11}	S_{DC12}
差分响应	Port 2	S_{DD21}	S_{DD22}	S_{DC21}	S_{DC22}
共模响应	Port 1	S_{CD11}	S_{CD12}	S_{CC11}	S_{CC12}
共模响应	Port 2	S_{CD21}	S_{CD22}	S_{CC21}	S_{CC22}



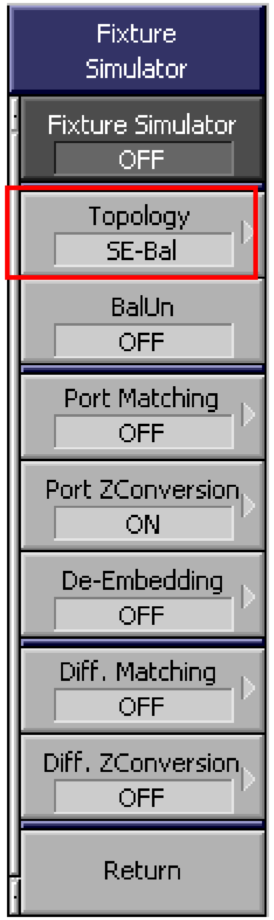
差分输入，共模响应
模式转换指标
反映器件产生干扰性能

共模输入，共模响应
反映器件共模性能

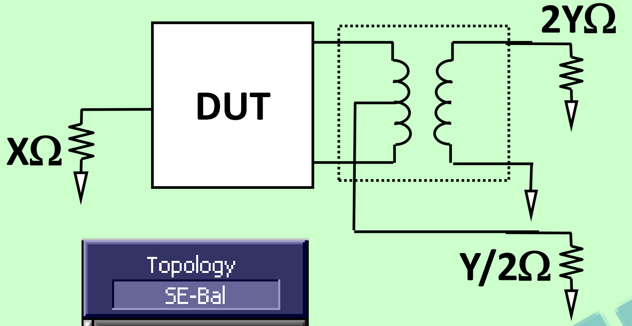


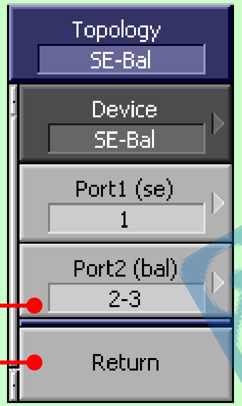
S=b/a 混合S参数定义: S 响应模式，激励模式，响应端口， 激励端口

平衡器件测试状态



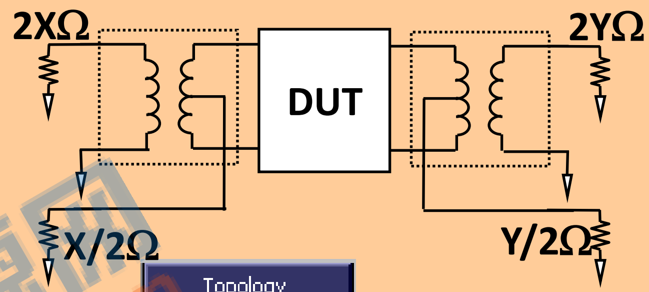
单端输入/差分输出





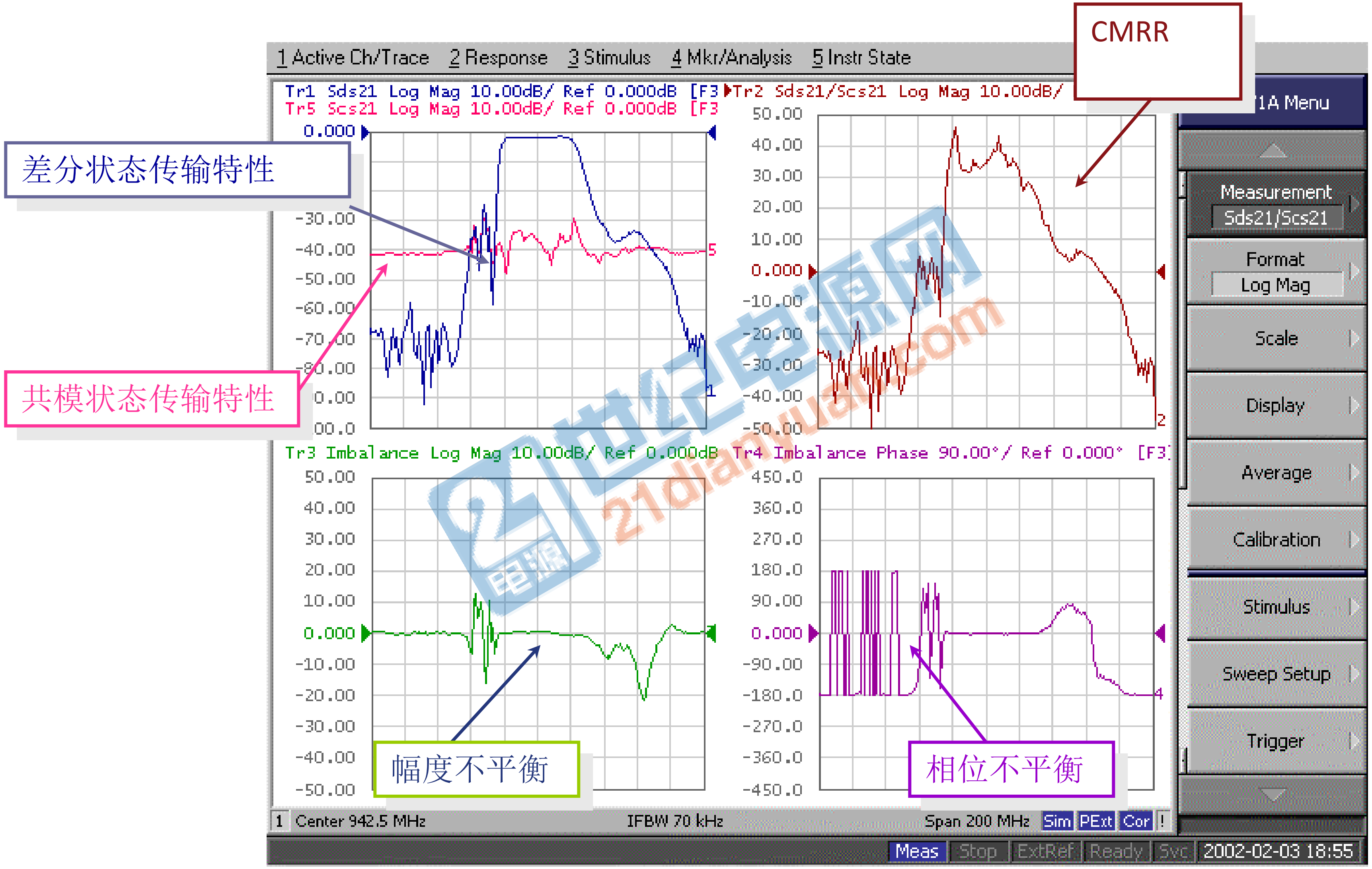
- 3个物理测试端口
- S参数测试：S11 ~ S33
- 2个逻辑测试端口
- 单端端口= 逻辑端口 1
- 平衡端口=逻辑端口 2
- 任何物理端口可被定义为单端口
- 任何两个物理端口可组合定义为平衡端口

差分输入/差分输出



- 4个物理测试端口
- S参数测试：S11 ~ S44
- 2个逻辑测试端口
- 平衡端口= 逻辑端口 1
- 平衡端口=逻辑端口 2
- 任何两个物理端口可组合定义为逻辑端口1
- 其余两个物理端口定义为逻辑端口2

ENA网络仪对平衡器件参数的测试



Keysight 精简系列VNA---新登场

简约造型，性能无损.

- Keysight 精简系列VNA，精巧造型易于运输（2端口VNA仅重2kg），可**单手携带**
- 和主控PC通过**USB或者雷电3**快速连接，易于设置
- 和Keysight 网分 (PNA, ENA, PXI VNA)使用相同测量科技，相同**用户界面GUI**，相同**SCPI程控命令集**
- 宽广的频率覆盖范围延申到**毫米波应用**（如5G FR2）
- 通过**级联两台VNA**可以扩展测试端口

精简系列VNA (B型) 基本特点

- 在不同地方的不同的用户可以很容易地远程共享仪器
- 利用PC 强大的硬件升级能力 (CPU, Memory等)
- 测试数据存储不在VNA. 易于数据安全性

- PC通过雷电3（Type-C连接器）电缆控制VNA.
- 不支持PC端的USB2.0/3.0连接控制VNA.
- VNA 固件需要Win-10 OS (64-bit)以上支持，启动精简型网分前，建议PC-BOIS对雷电控制器驱动等都升级到最新版
- ECal 电子校准件可以连接到PC或者VNA的 USB2.0 端口

合成两台网分得到更多测试端口

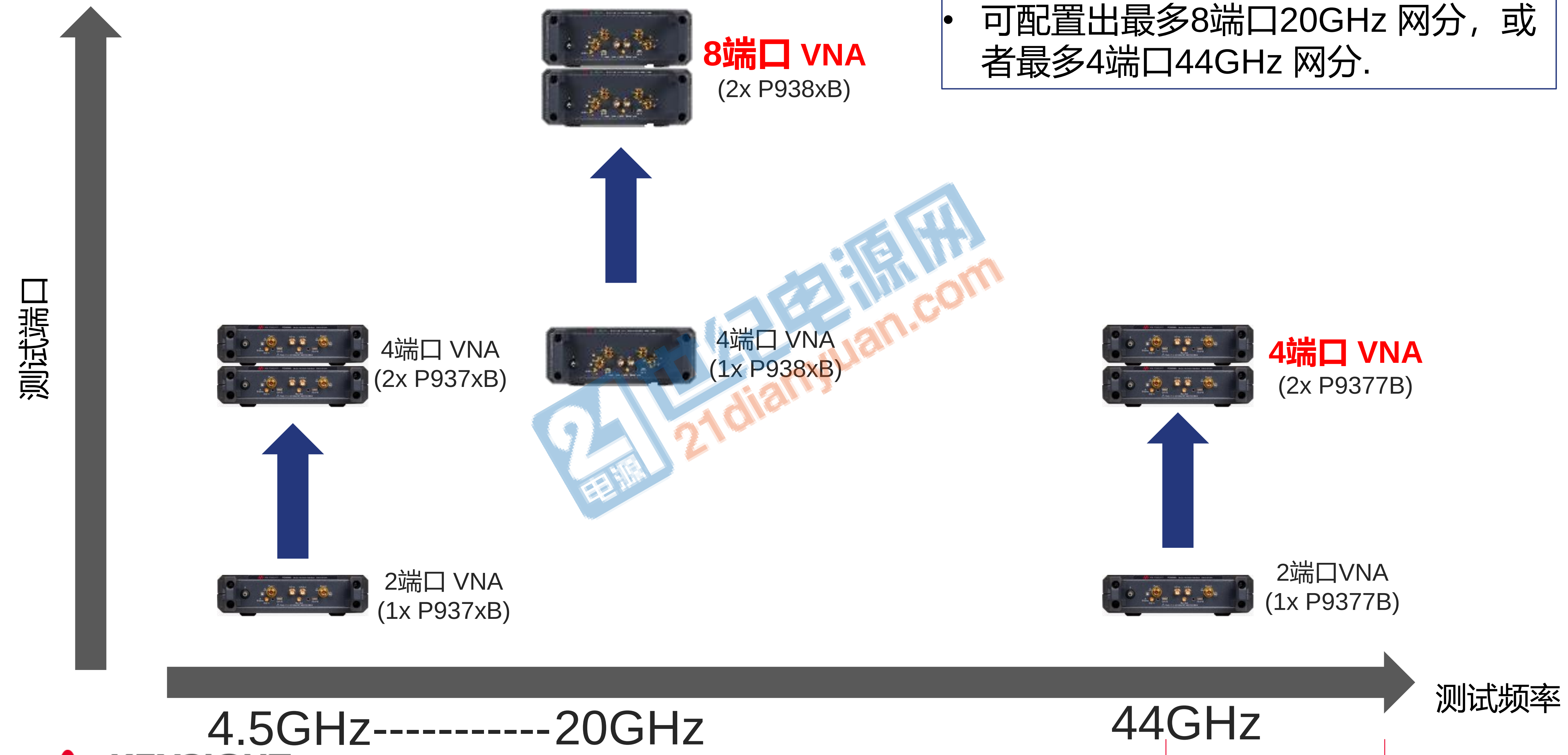
- 通过级联两台网分扩展测试端口.
- 两台网分用Y1701A电缆套件互联就可以配置出一个多端口网分.
- 使用S97551B软件可以进行多端口校准

2端口 P937xB + 4端口 P938xB = **6端口 VNA**

- 其中一台网分要安装S97551B 软件, 多仪器校准测量软件.
- 每台 P93xxB VNA 标配一根0.8m雷电3控制连接电缆 (0.8 m, Keysight型号Y1701A-400) .
- 主控PC需要直接的雷电3 (USB Type-C)接口连接到仪器，不支持通过USB3.0 转接到雷电3.
- 推荐使用4端口电子校准件Ecal如N4433D 或者 N4431D 用于多端口仪器校准.

合成两台网分得到更多测试端口

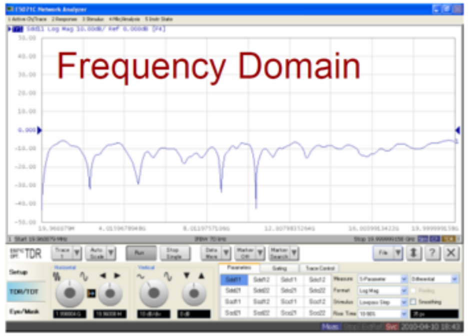
- 可配置出最多8端口20GHz 网分，或者最多4端口44GHz 网分.

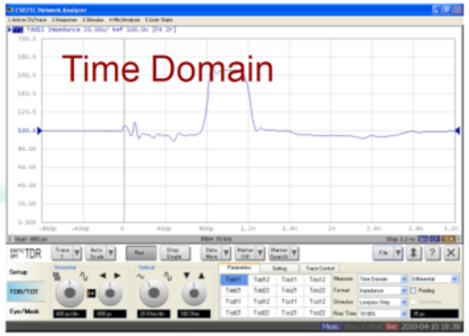


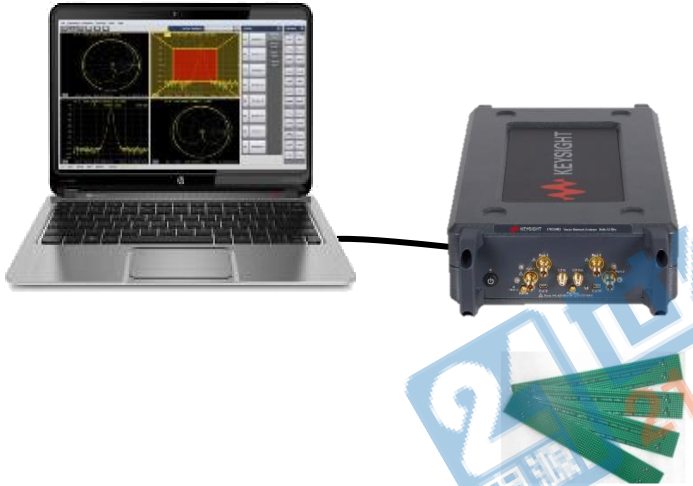
应用案例------数字线缆以及柔性PCB测试

时域和频域测试

P93xxB 简约网分 + S97011B 增强时域分析TDR软件







- 被测物DUT: PCB硬板和PCB挠性板(flexible PCB 或者 FPC)
- 行业: 电子器件, 手机, 物联网, 汽车电子
- 测试参数: 差分阻抗(**Tdd11**), 差分回损(**Sdd11/22**), 差分插损(**Sdd21**)等

测量挑战和需求:

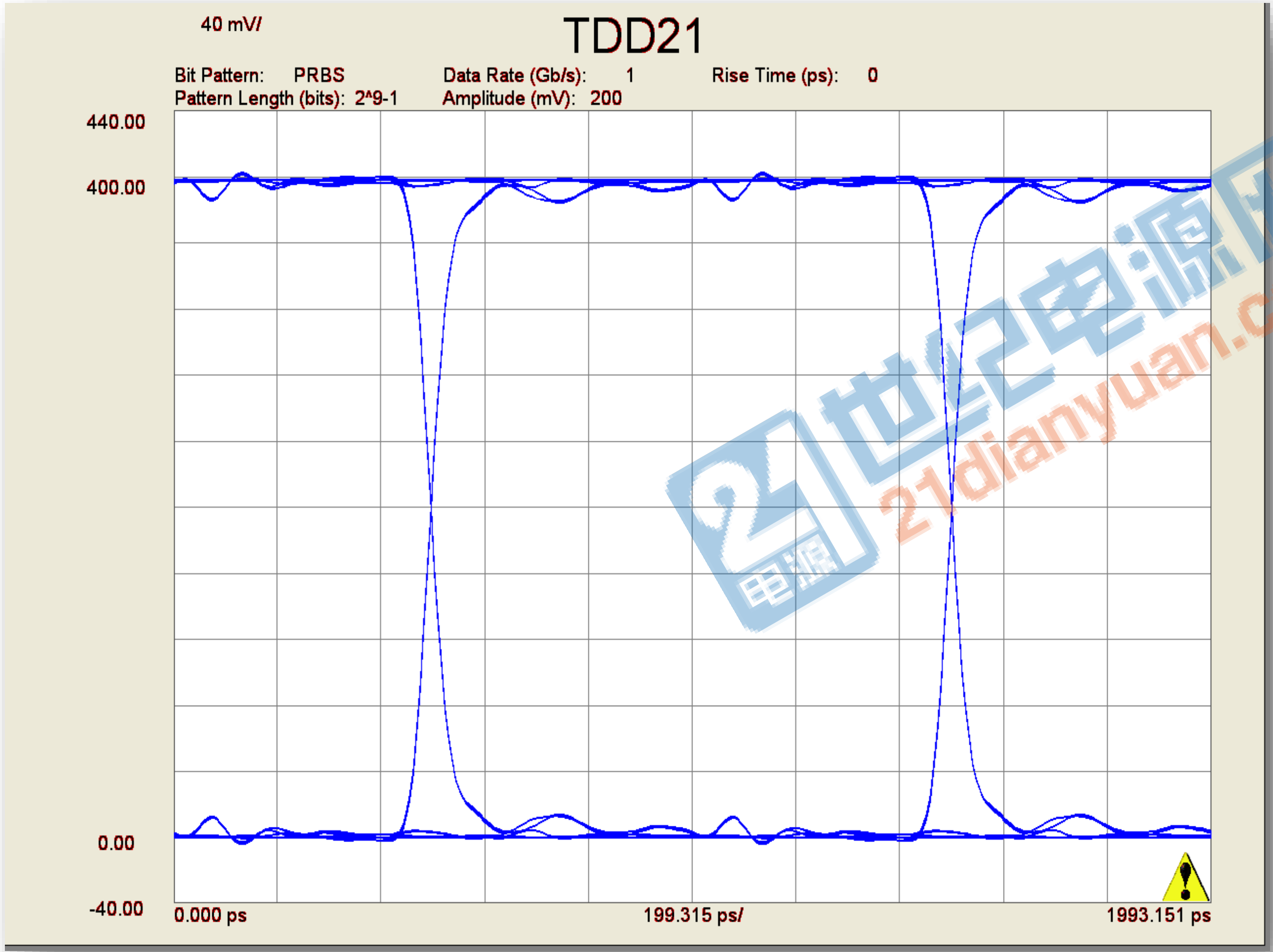
- **多端口** = 差分输入和差分输出端口 (4个单端口)
- 时域(阻抗) 和频域(S参数) 测量
- 宽频(以获取更窄时域分辨率)
- 较低维护成本

Keysight产品优势

1. **4端口**矢量网分 (**P9384B达到20GHz**，或者**2台P9377B +S97551B**拼接软件达到**44GHz**)
2. 使用增强时域分析软件S97011B 无缝测量TDR
3. 使用ECal校准进行高精度测量
4. VNA架构抗强ESD静电

– 实操演示和问题解答

TDD21 Eye Diagram



Name	Measurement Result
Eye Level Zero(mV)	2.19
Eye Level One(mV)	395.94
Eye Level Mean(mV)	199.06
Eye Amplitude(mV)	393.75
Eye Height(mV)	373.83
Eye Height(db)	-4.27
Eye Width	1.00e-009
Eye Opening Factor	0.95
Eye Signal_to_Noise	68.96
Eye Duty Cycle Dist	6.31e-014
Eye Duty Cycle Dist(%)	0.01
Eye Rise Time (20-80)	4.99e-011
Eye Fall Time (80-20)	4.99e-011
Eye Jitter(PP)	0.00e+000
Eye Jitter(RMS)	0.00e+000

ENA-C TDR Diff Eye Domain – Tdd21 1Gbps

# E5071C ENA Option TDR Simulated Eye Results	
# 11/24/2011 2:02:52 AM	
#	
Level Zero (V)	0.031792681
Level One (V)	0.342192319
Level Mean (V)	0.1869925
Amplitude (V)	0.310399638
Height (V)	0.194655882
Width (s)	9.40E-10
Opening Factor	0.875704585
Signal / Noise	8.045349026
Duty Cycle Distortion	9.54E-14
Duty Cycle Distortion (%)	0.009540651
Rise Time (s)	4.26E-10
Fall Time (s)	4.25E-10
Jitter (PP)	4.06E-11
Jitter (RMS)	9.98E-12
Cross Point (%)	49.97999512

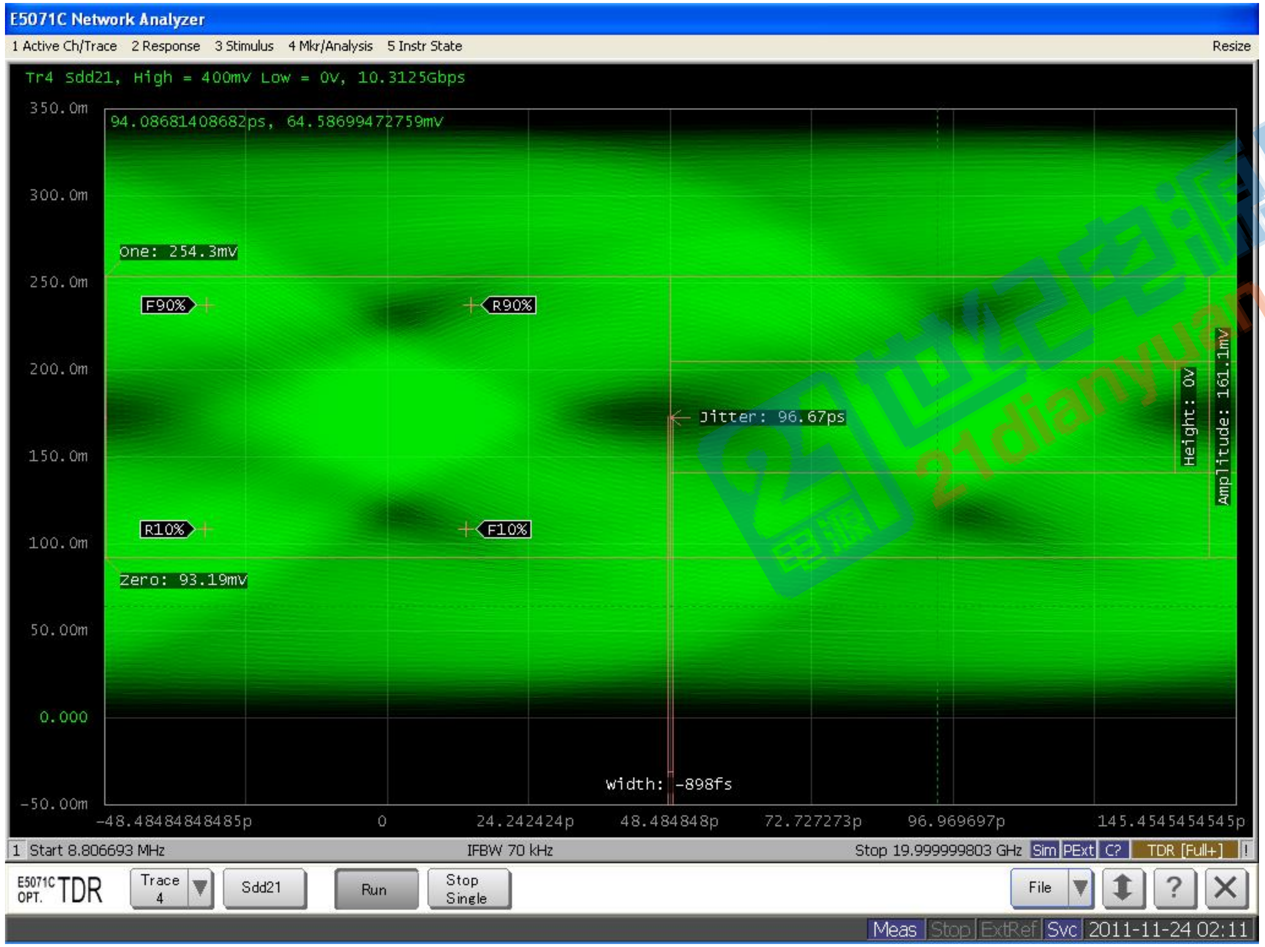
ENA-C TDR Diff Eye Domain – Tdd21 3.125Gbps

# E5071C ENA Option TDR Simulated Eye Results	
# 11/24/2011 2:04:11 AM	
#	
Level Zero (V)	0.053826879
Level One (V)	0.306752666
Level Mean (V)	0.180289772
Amplitude (V)	0.252925787
Height (V)	0.07153229
Width (s)	2.47E-10
Opening Factor	0.760939762
Signal / Noise	4.183046116
Duty Cycle Distortion	9.10E-13
Duty Cycle Distortion (%)	0.28424748
Rise Time (s)	2.23E-10
Fall Time (s)	2.25E-10
Jitter (PP)	4.70E-11
Jitter (RMS)	1.22E-11
Cross Point (%)	49.9584342

KEYSIGHT TECHNOLOGIES

ENA-C TDR Diff Eye Domain – Tdd21 10.3125Gbps

Without Equalization

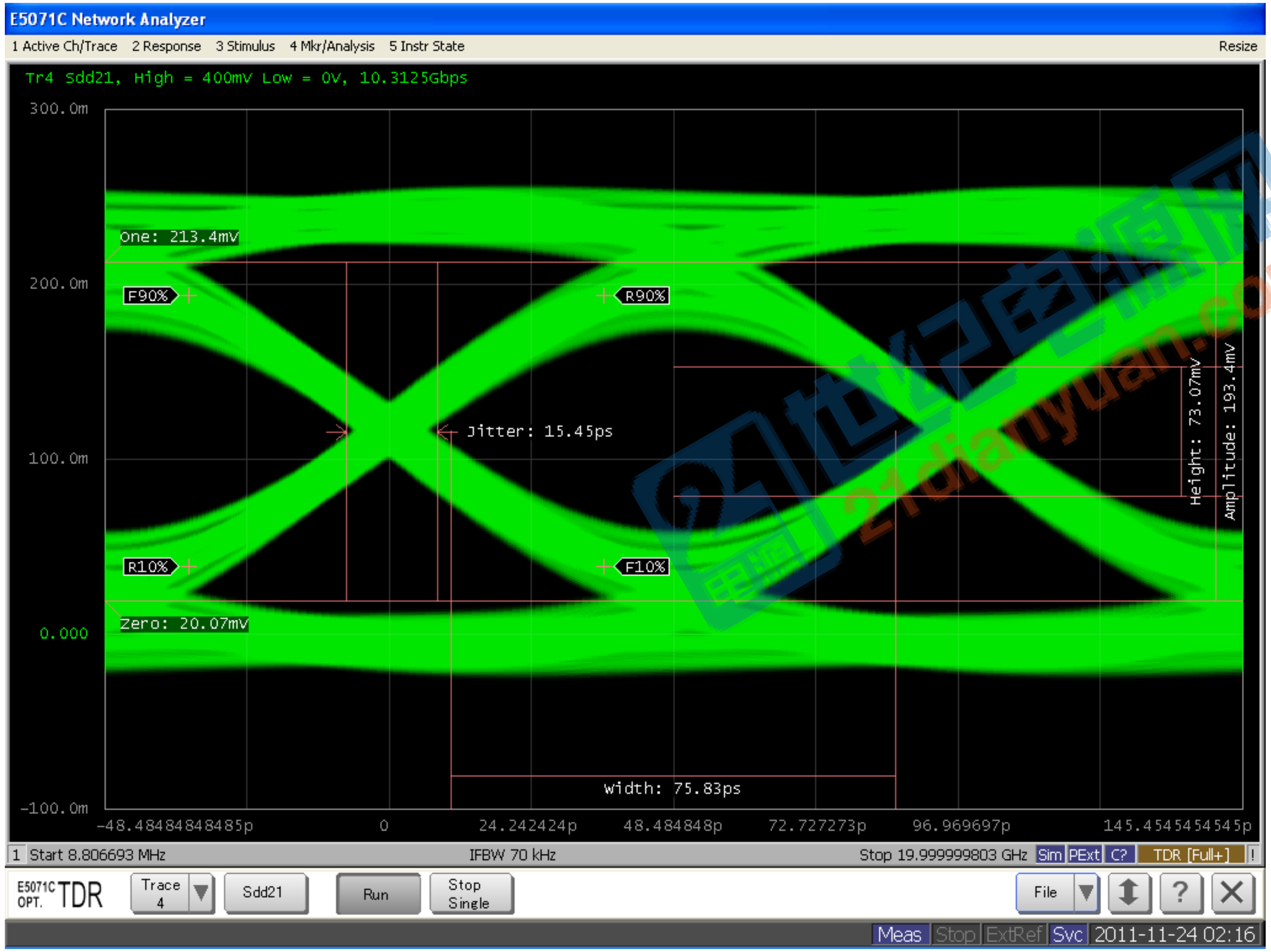


# E5071C ENA Option TDR Simulated Eye Results	
# 11/24/2011 2:12:27 AM	
#	
Level Zero (V)	0.093189224
Level One (V)	0.254257415
Level Mean (V)	0.173723319
Amplitude (V)	0.16106819
Height (V)	0
Width (s)	-8.98E-13
Opening Factor	0.533893954
Signal / Noise	2.145434519
Duty Cycle Distortion	2.11E-13
Duty Cycle Distortion (%)	0.217549314
Rise Time (s)	4.54E-11
Fall Time (s)	4.44E-11
Jitter (PP)	9.67E-11
Jitter (RMS)	1.63E-11
Cross Point (%)	50.0671134

KEYSIGHT TECHNOLOGIES

ENA-C TDR Diff Eye Domain – Tdd21 10.3125Gbps

With Equalization



# E5071C ENA Option TDR Simulated Eye Results	
# 11/24/2011 2:17:15 AM	
#	
Level Zero (V)	0.020071422
Level One (V)	0.213444394
Level Mean (V)	0.116757908
Amplitude (V)	0.193372972
Height (V)	0.073065135
Width (s)	7.58E-11
Opening Factor	0.792615214
Signal / Noise	4.821954497
Duty Cycle Distortion	1.16E-14
Duty Cycle Distortion (%)	0.011993989
Rise Time (s)	7.06E-11
Fall Time (s)	7.07E-11
Jitter (PP)	1.55E-11
Jitter (RMS)	3.52E-12
Cross Point (%)	49.99968324

谢谢！

Thank You！