



电动汽车LLC电路磁元件分析与设计

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中国电源学会磁技术专委会副主任委员兼副秘书长

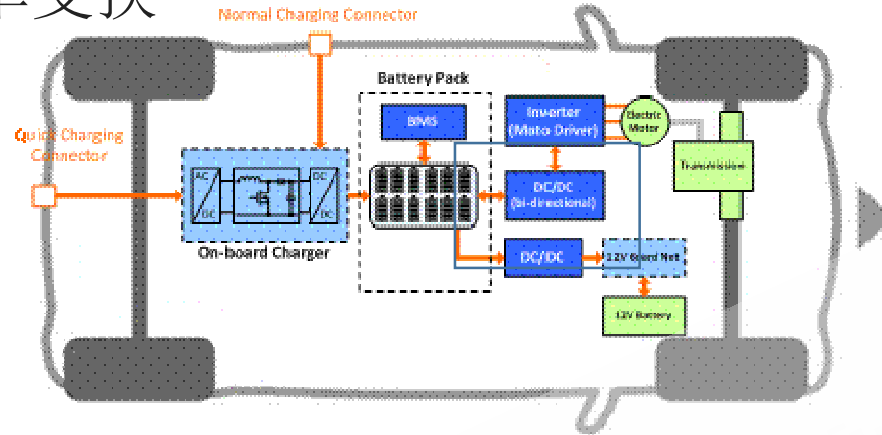
全国磁性元件与铁氧体材料标准化技术委员会(磁标委)委员

2020年04月16日

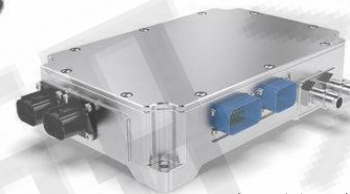


- 电动汽车充电系统中的磁性元件
- LLC变压器的损耗优化设计
- LLC变压器绕组交流电阻测试方法
- LLC变压器的EMI优化设计
- LLC变压器EMI性能的评估方法

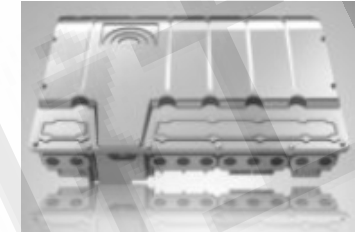
功率变换



双向DC/DC变换器

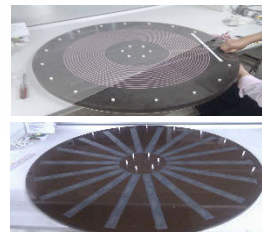
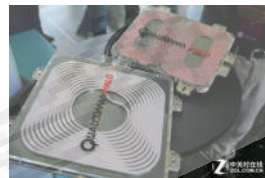
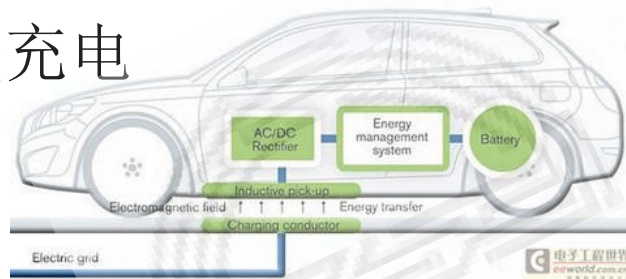


车载充电机

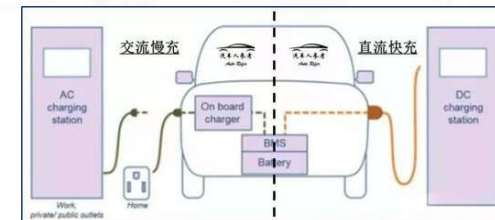


电控逆变器

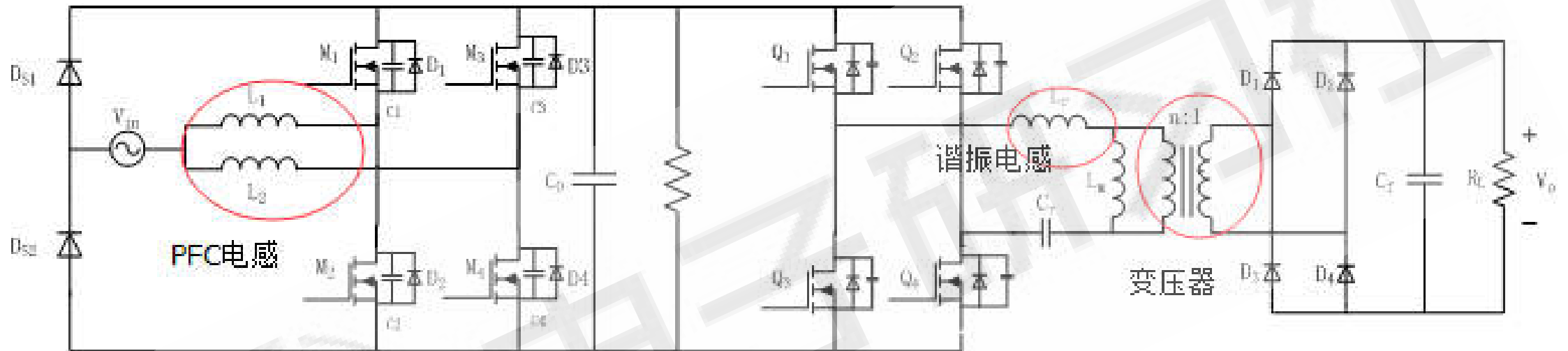
无线充电



有线充电



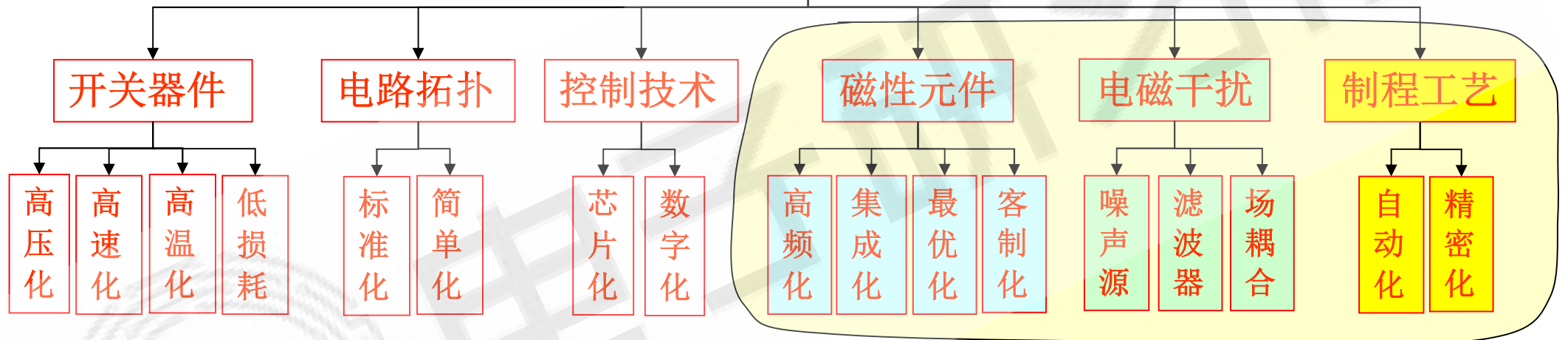
□ 新能源汽车已成为磁性元件、磁材料企业的重点关注项目



交错并联图腾柱无桥PFC

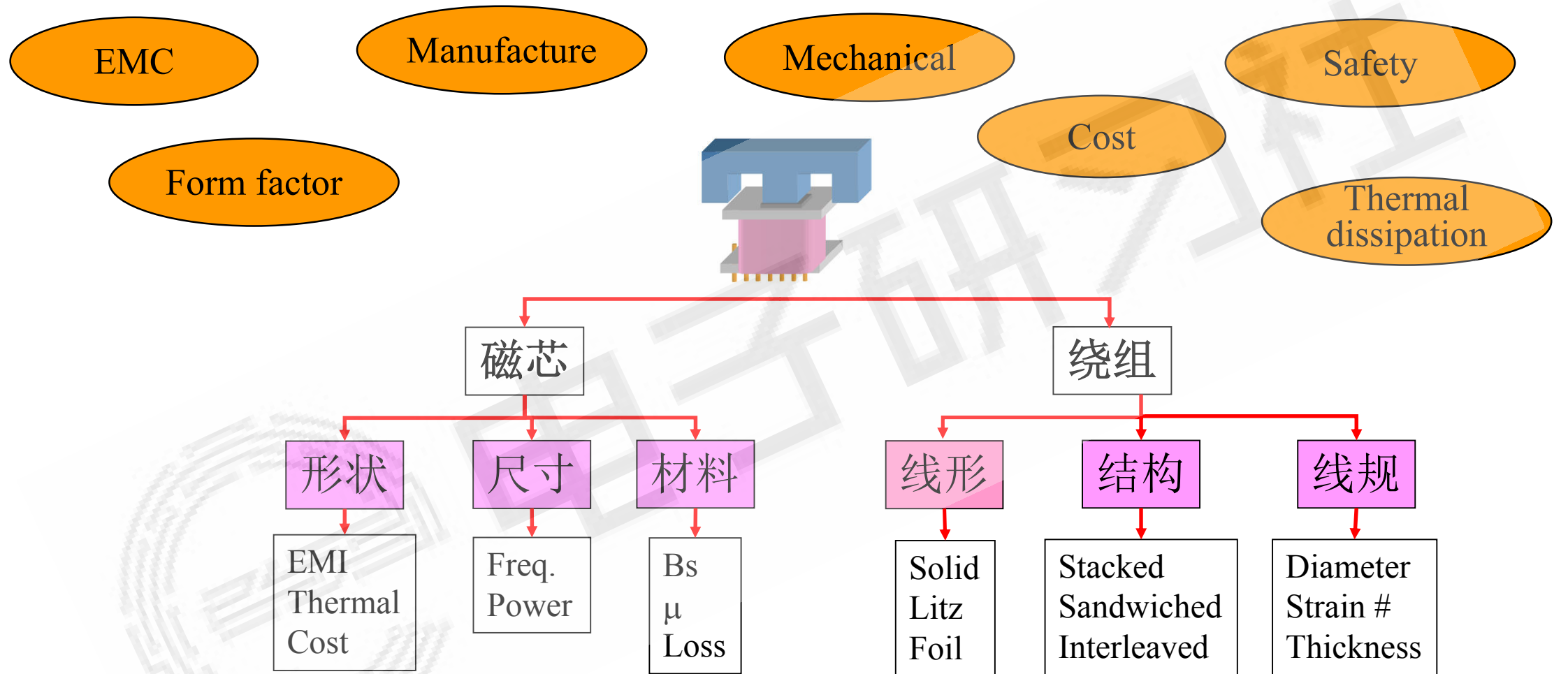
全桥LLC谐振变换器

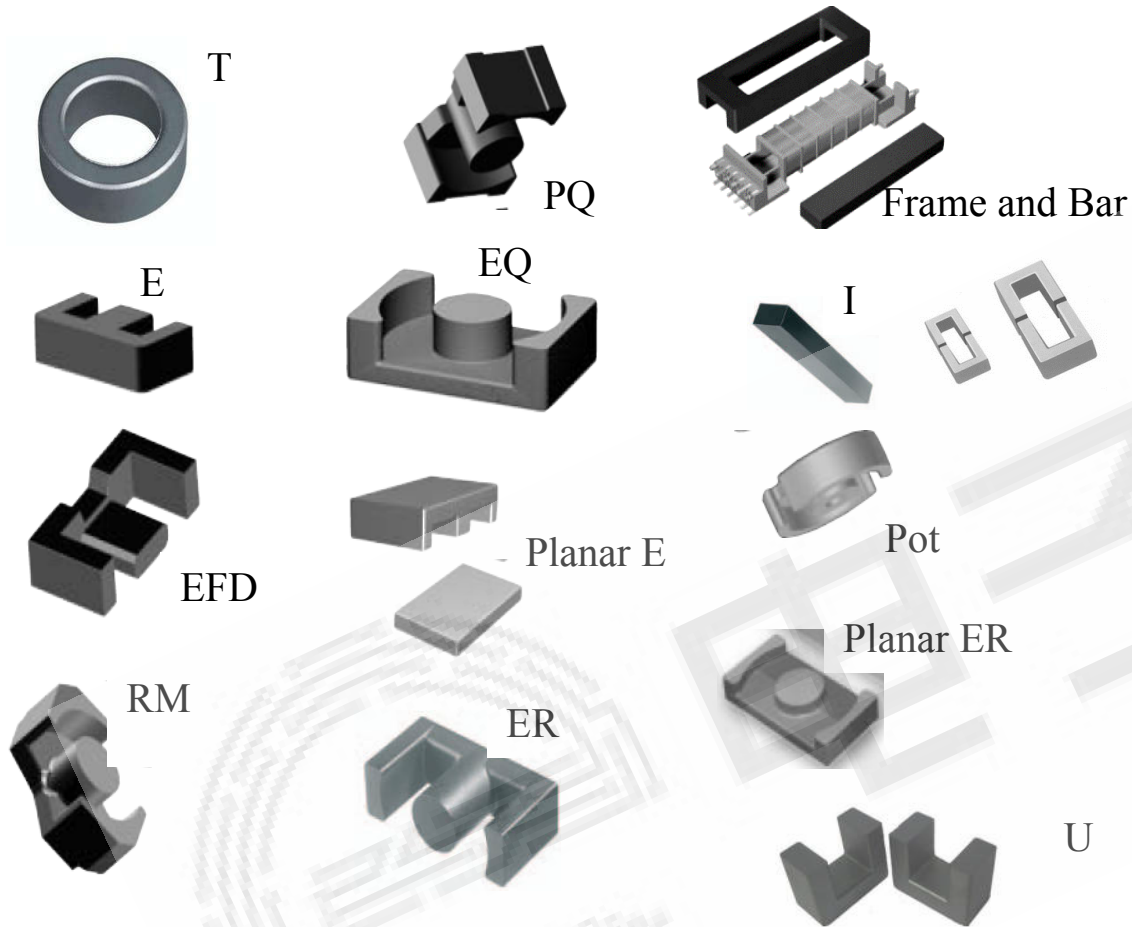
高效率，高密度，高可靠，低价格，低高度



与磁元件都有密切关系

□ 随着宽禁带器件的应用，高频化趋势使得磁元件越显重要

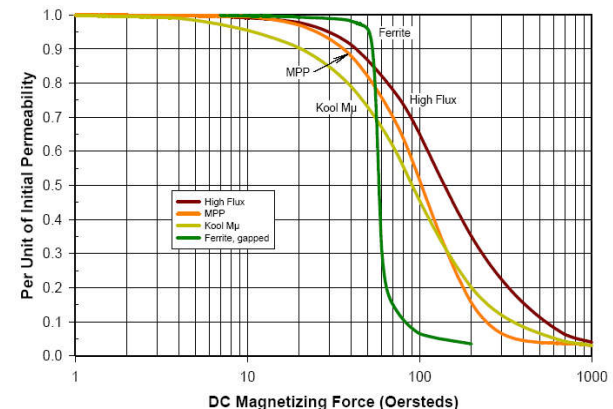
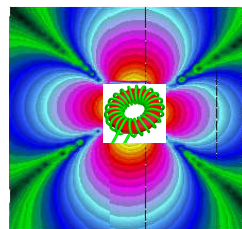
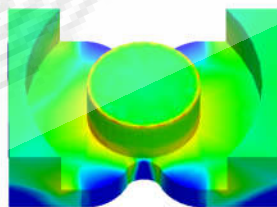
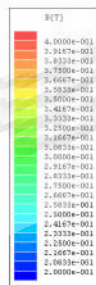
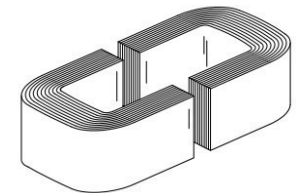
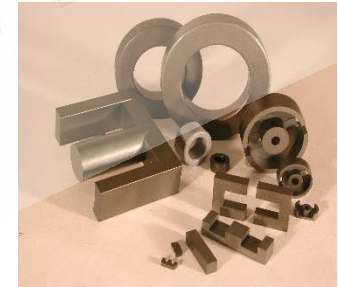




磁合金粉材
 Fe (铁粉芯)
 MPP (铁镍铝合金)
 High Flux (高磁通铁镍)
 Kool Mu (铁硅铝合金)
 Fe-Si (铁硅合金)

铁氧体块材
 Mn-Zn
 Ni-Zn

磁合金带材
 Silicon steel (硅钢片)
 Permalloy (坡莫合金)
 Amorphous (非晶)



圆电磁线



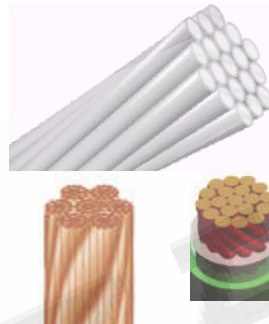
方电磁线



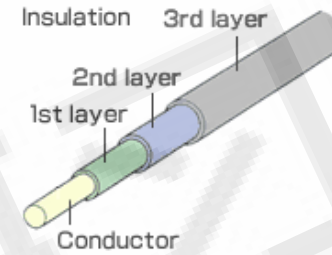
铜箔导体



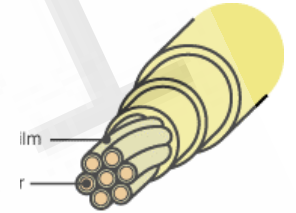
多股绞线



三层绝缘线



三层绝缘绞线



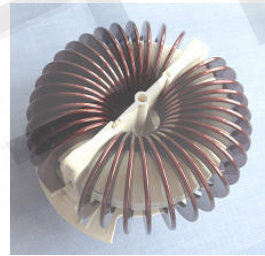
PCB绕组



扁螺旋立绕线圈



垂直环形立绕绕组



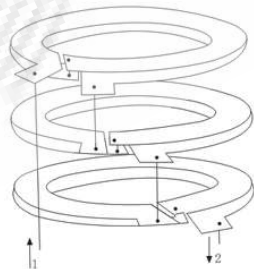
螺旋线



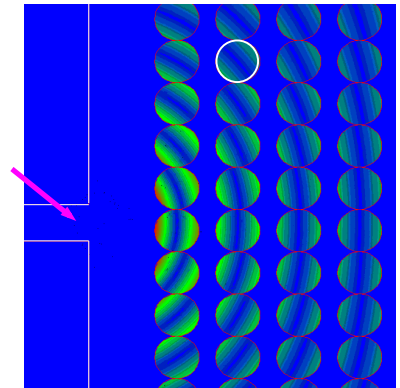
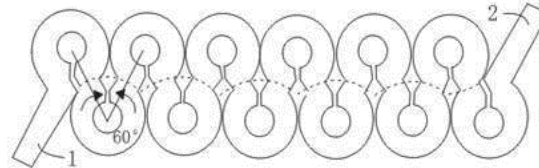
自粘漆包线



冲叠绕组



折叠绕组





$$AP = A_e A_w$$

基于传输容量

磁芯尺寸

变压器

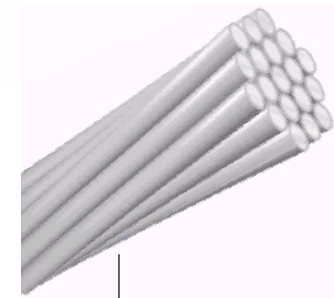
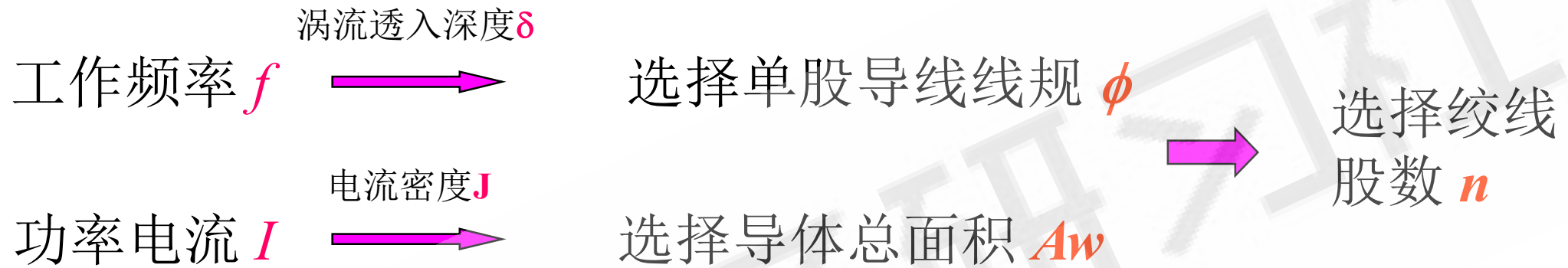
$$\begin{aligned} AP &= A_e \cdot A_w \\ &= \frac{V\Delta t}{2B_{ac}N} \cdot \frac{N_p I_{prms} + N_s I_{srms}}{JK_u} \\ &= \frac{V_{pk}D}{2B_{ac}fN_p} \cdot \frac{N_p I_{prms}}{JK_u} + \frac{V_{spk}(1-D)}{2B_{ac}fN_s} \cdot \frac{N_s I_{srms}}{JK_u} \\ &= \frac{V_{pk}DI_{prms} + V_{spk}(1-D)I_{srms}}{2f \cdot B_{ac}J \cdot K_u} \end{aligned}$$

电感器

$$\begin{aligned} AP &= A_e \cdot A_w \\ &= \frac{L \left(I_{dc} + \frac{\Delta I}{2} \right) NI_{rms}}{NB_{max} JK_u} \\ &= \frac{\sqrt{2}LI_{rms}^2 \left(1 + \frac{K_{rp}}{2} \right)}{B_{max}J \cdot K_u} \end{aligned}$$

主要局限:

- 1、 B 和 J 难以预先给定，尤其是 J
- 2、是基于电磁参数的可行选择，不是基于损耗的设计
- 3、是基于经验手册的估计选择，不是基于优化的设计
- 4、是选择磁芯尺寸大小的方法，不是设计磁芯。



主要局限:

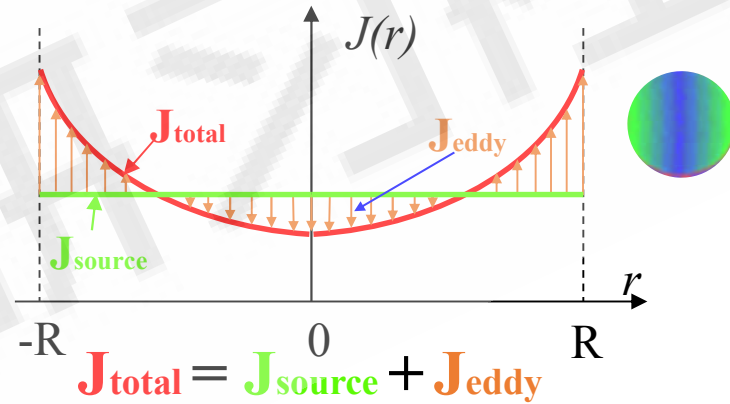
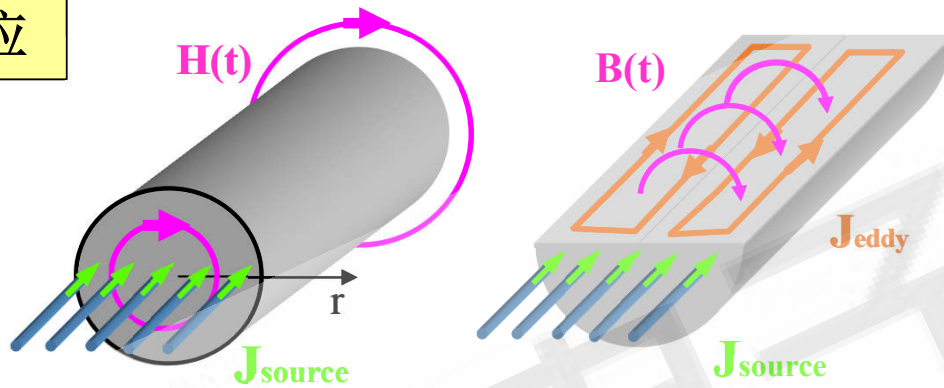
- 1、对铜箔导体，在一定空间下，选择尽可能厚的铜箔；
- 2、对多股绞线，在一定股径下，选择尽可能多的股数。

电磁感应定律

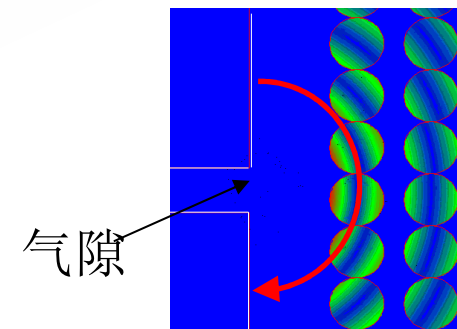
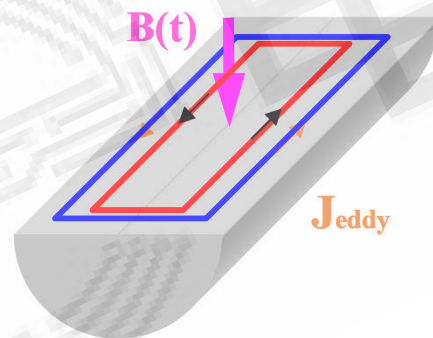
$$E = -\frac{d\Phi}{dt}$$

涡流效应

集肤效应



邻近效应



- 涡流效应导致电流密度分布不均匀，从而引起损耗增加，
- 涡流效应引起进入导体磁通被抵消，从而引起磁通下降。

$$\nabla \times H = J$$



$$\nabla \times \nabla \times H = \nabla \times J$$

$$\nabla \times E = -\frac{\partial B}{\partial t}$$



$$\nabla \times J = -j\omega\sigma\mu H$$

$$B = \mu H$$

$$J = \sigma E$$

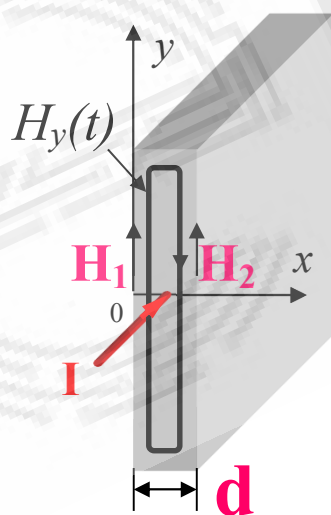
$$\nabla \cdot B = 0$$

$$\nabla^2 \vec{H} - j\omega\sigma\mu \vec{H} = 0$$

其中: $\vec{H} = H_x(x, y, z)\mathbf{i} + H_y(x, y, z)\mathbf{j} + H_z(x, y, z)\mathbf{k}$

$$\nabla \times \nabla \times H = \nabla(\nabla \cdot H) - \nabla^2 H \quad \longrightarrow \quad \nabla \times \nabla \times H = -\nabla^2 H$$

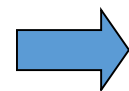
对于一维简化模型: $\vec{H} = H_y(x)$



$$\frac{\partial^2 H_y(x)}{\partial x^2} - j\omega\sigma\mu H_y(x) = 0$$

With $H_y(x=0) = H_1$

$H_y(x=d) = H_2$

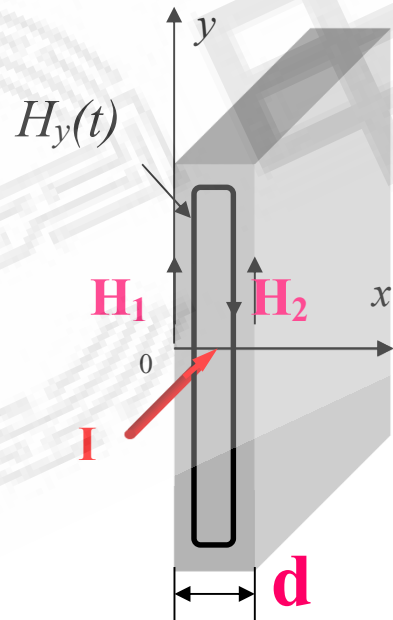
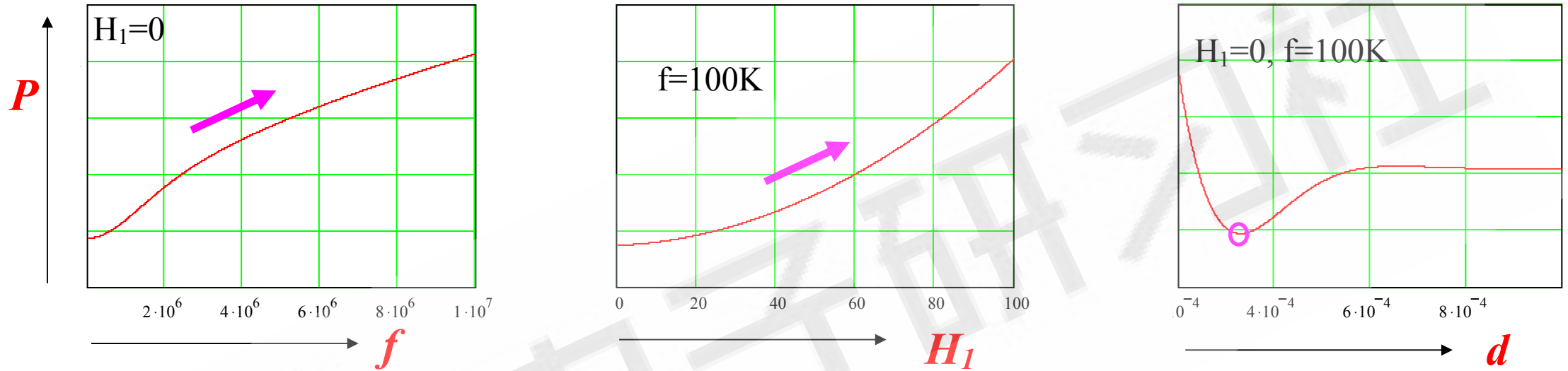


$$H_y(x) = \frac{H_1 \sinh[k(d-x)] + H_2 \sinh(kx)}{\sinh(kd)}$$

$$J_y(x) = k \cdot \frac{H_1 \cosh[k(d-x)] - H_2 \cosh(kx)}{\sinh(kd)}$$

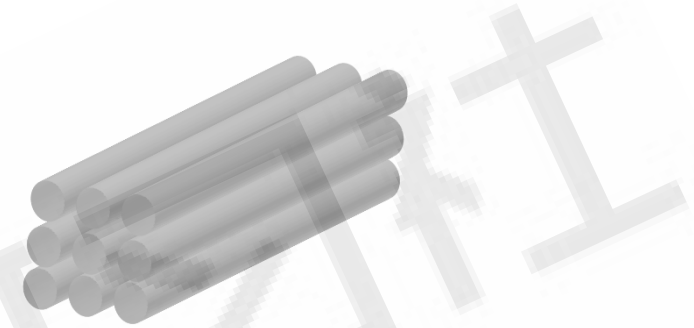
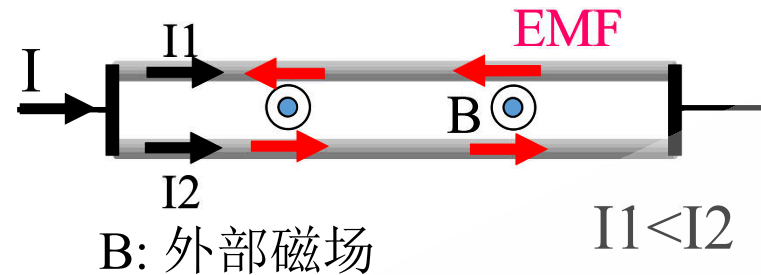
$$k = \sqrt{j\omega\sigma\mu} = \sqrt{j2\pi f\sigma\mu}$$

$$P = \frac{MLT \cdot A}{2\sigma} \int_0^d |J_y(x)|^2 dx$$

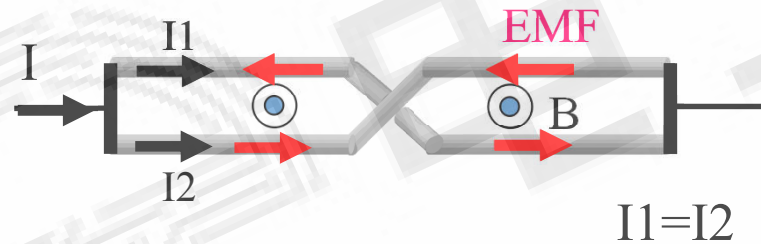


- 绕组交流电阻随频率的提高而增大；
- 绕组交流电阻随所处磁场强度的增大而增大；
- 绕组交流电阻随铜箔宽度/导线线径变化存在一个最小损耗点。

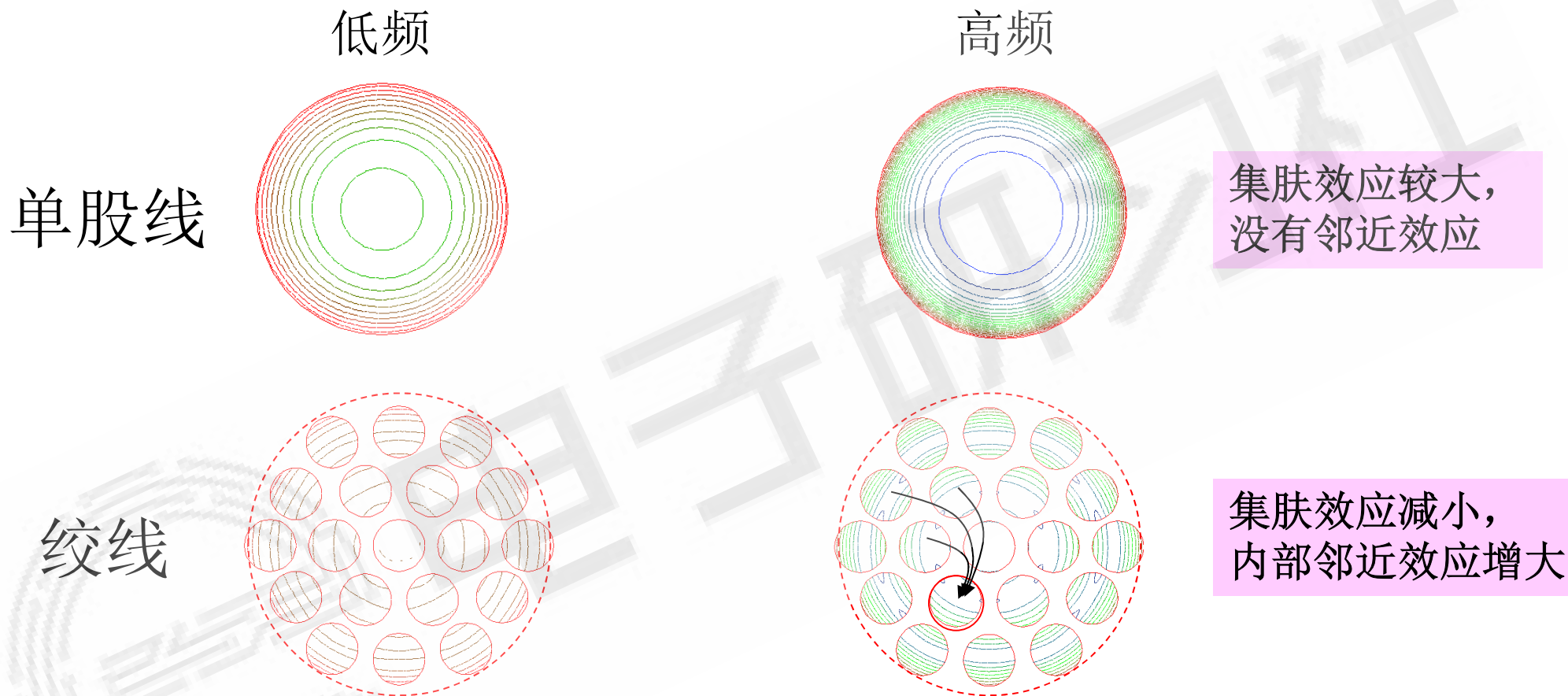
没有绞的多股并联导线



有绞的多股并联导线



里兹线参数：股径，股数，绞距，绞制方式。



集肤效应较大，
没有邻近效应

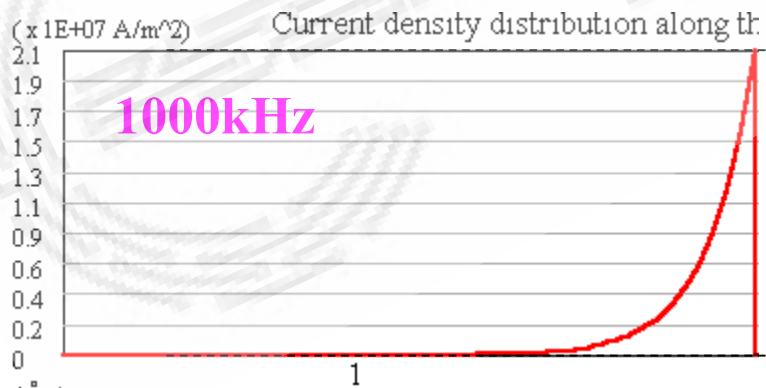
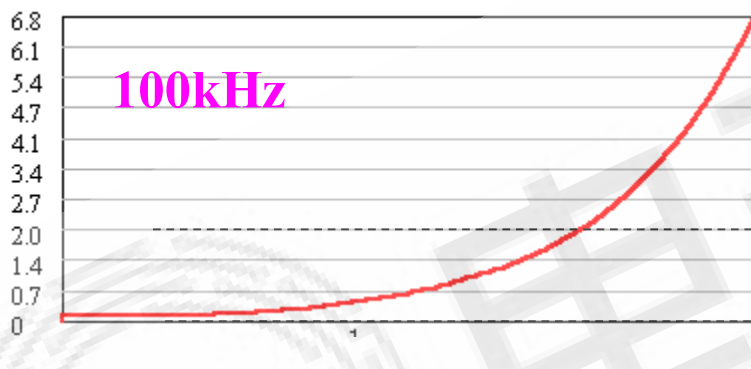
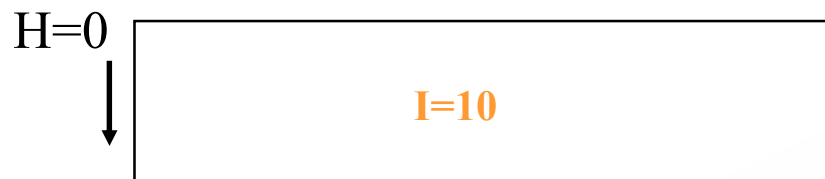
集肤效应减小，
内部邻近效应增大

对多股绞线的每一股来说，集肤效应大大减弱了，但存在其它股电流对其的邻近效应（内部邻近效应）。股数越多，内部邻近效应越强。

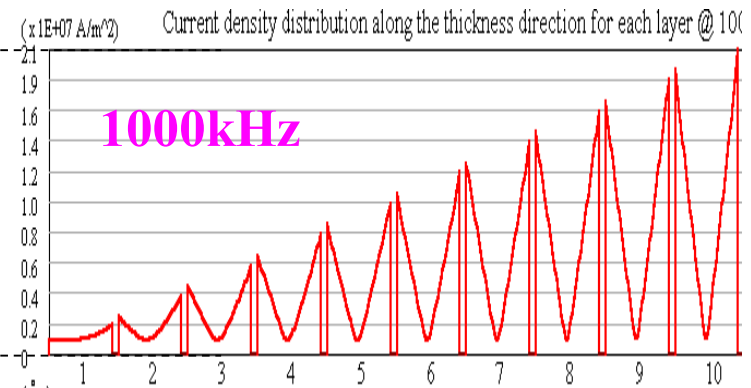
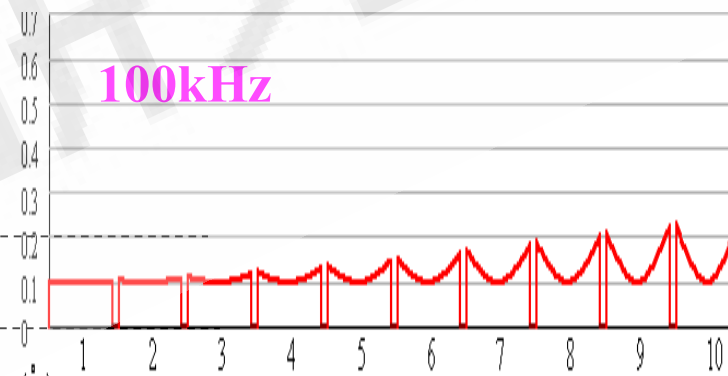


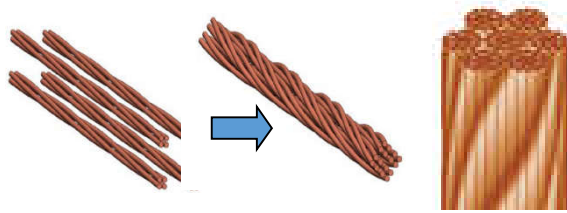
多股绞线涡流分布比较

单股线 (1.0mm*1股)



绞线(0.1mm*100股)



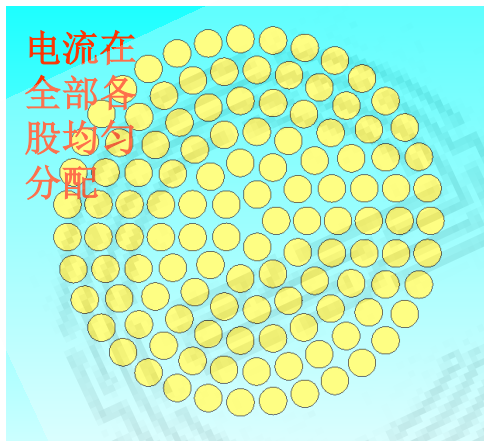


□ 复合绞线

(Rope Lay strained wire of Litz)

Size (AWG/MCM)	Construction Number of Wires /inch	Conductor Diameter Approx.		Weight Approximate	
		(inches)	(mm)	lb/1000ft	kg/km
8	7x270.010	0.18	4.55	59	88
7	7x310.010	0.19	4.88	68	101
6	7x380.010	0.21	5.40	83	124

abcwire.com

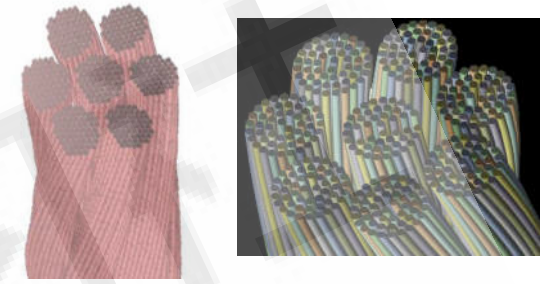
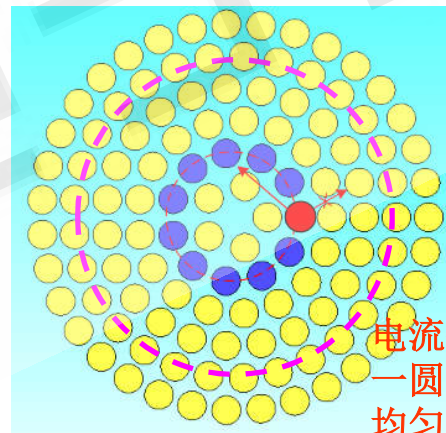


□ 同心绞线

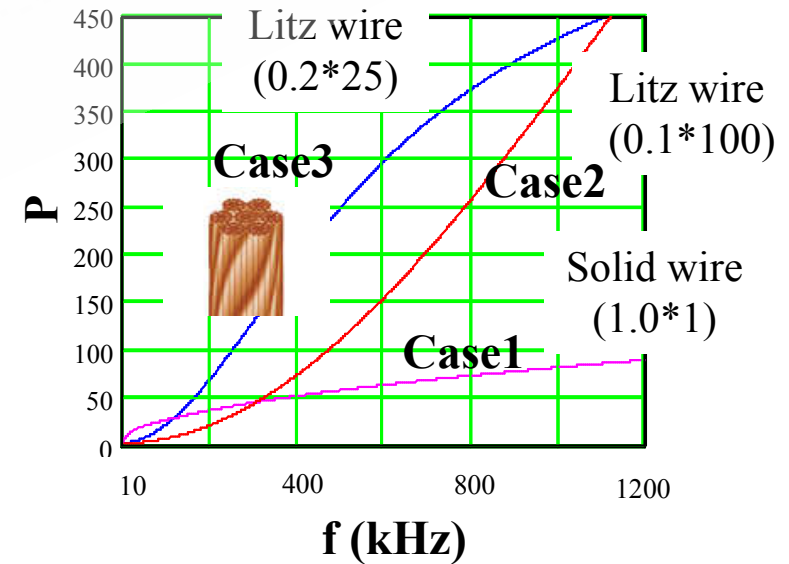
(Bunch strained wire of Litz)

EQUIV. AWG	CORE O.D. (in)	CIR. MILS	NO. STRANDS	AWG OF STRANDS	NOMINAL O.D. (in)	SUGGESTED OPERATING FREQUENCY
12	0.0950	5600	350	38	0.1070	400-850 khz
12	0.0950	5600	350	38	0.1130	400-850 khz
11	0.0844	3300	825	44	0.0964	400-850 khz
11	0.0844	3300	825	44	0.1024	400-850 khz

Rubadue.com

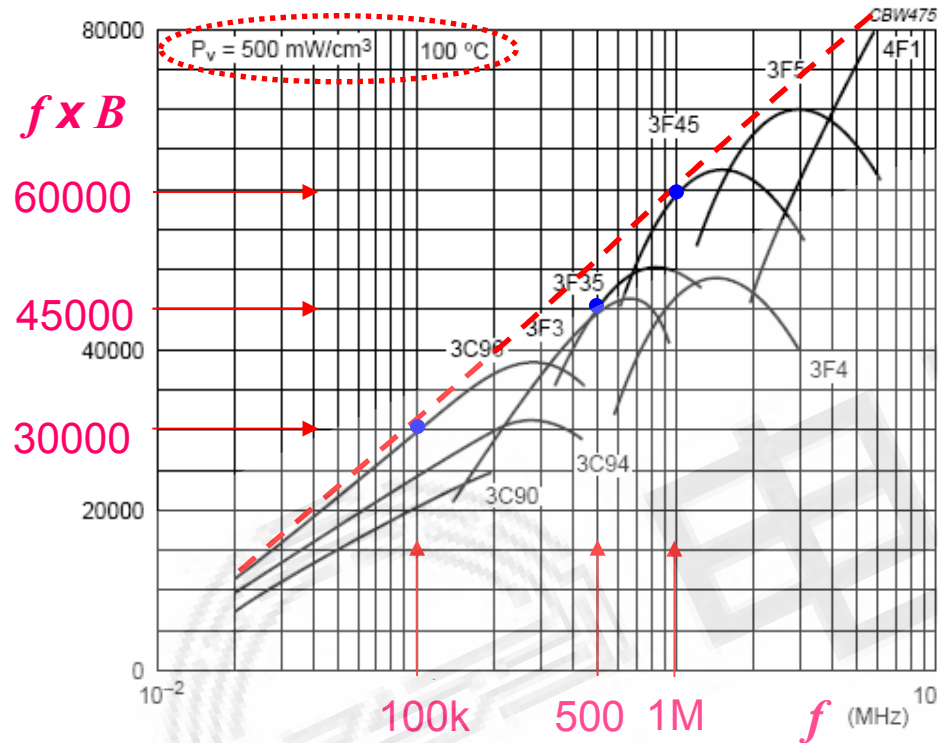


前两种的综合

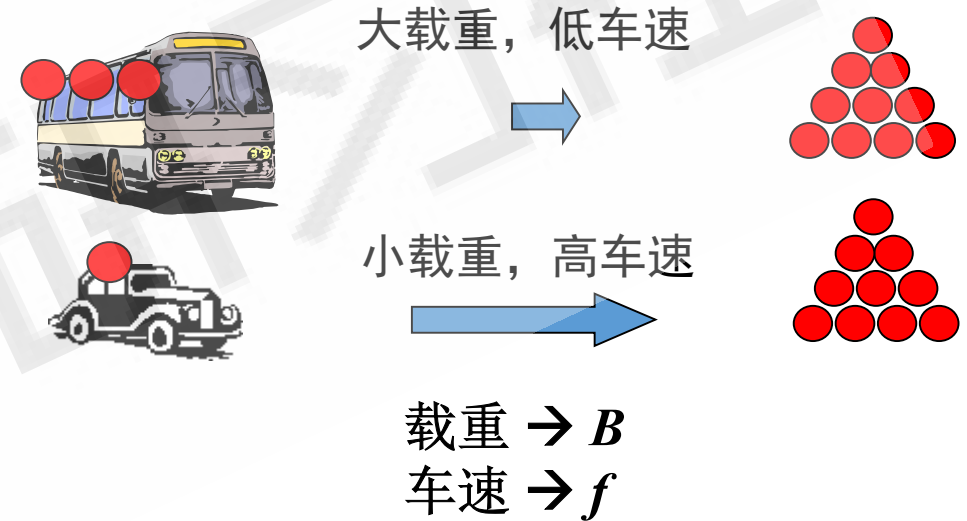


- 频率提高 → Litz线广泛应用，且线规选择更加重要
- 对于复合绞线，有计算/仿真模型，线规选择基本有依据
- 但对于同心绞线，目前还没有计算模型，损耗难以评估

$f \times B$: 在一定功耗下传输磁能的能力



$$S = UI = 4.44 \cdot f \cdot (N \cdot A) \cdot B \cdot I$$

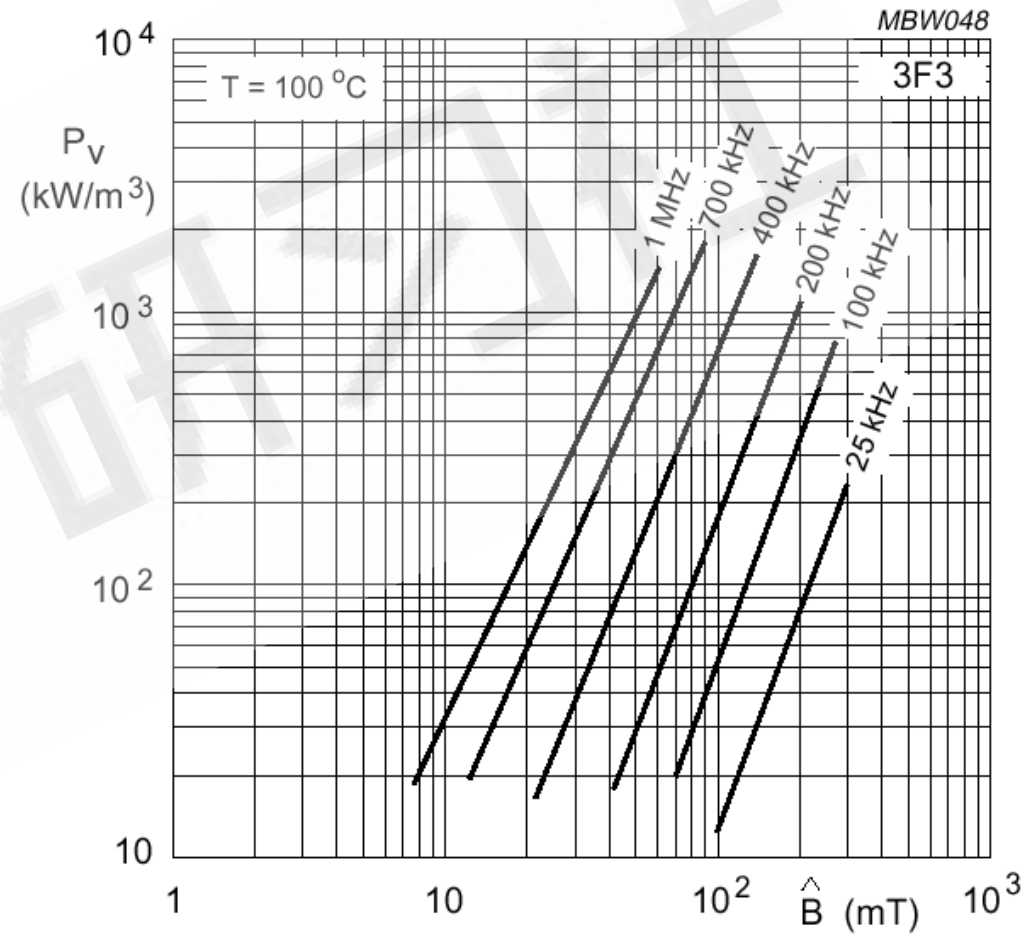
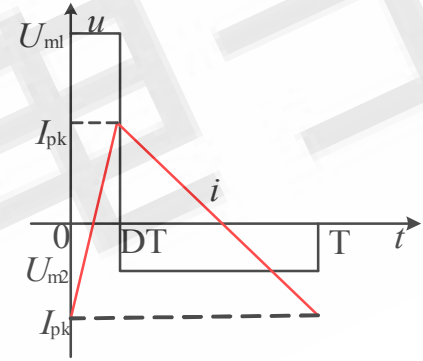
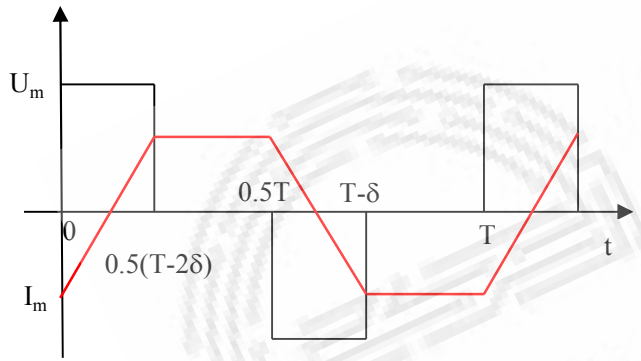


在低频下：饱和是主要限制因素
在高频下：损耗是主要限制因素

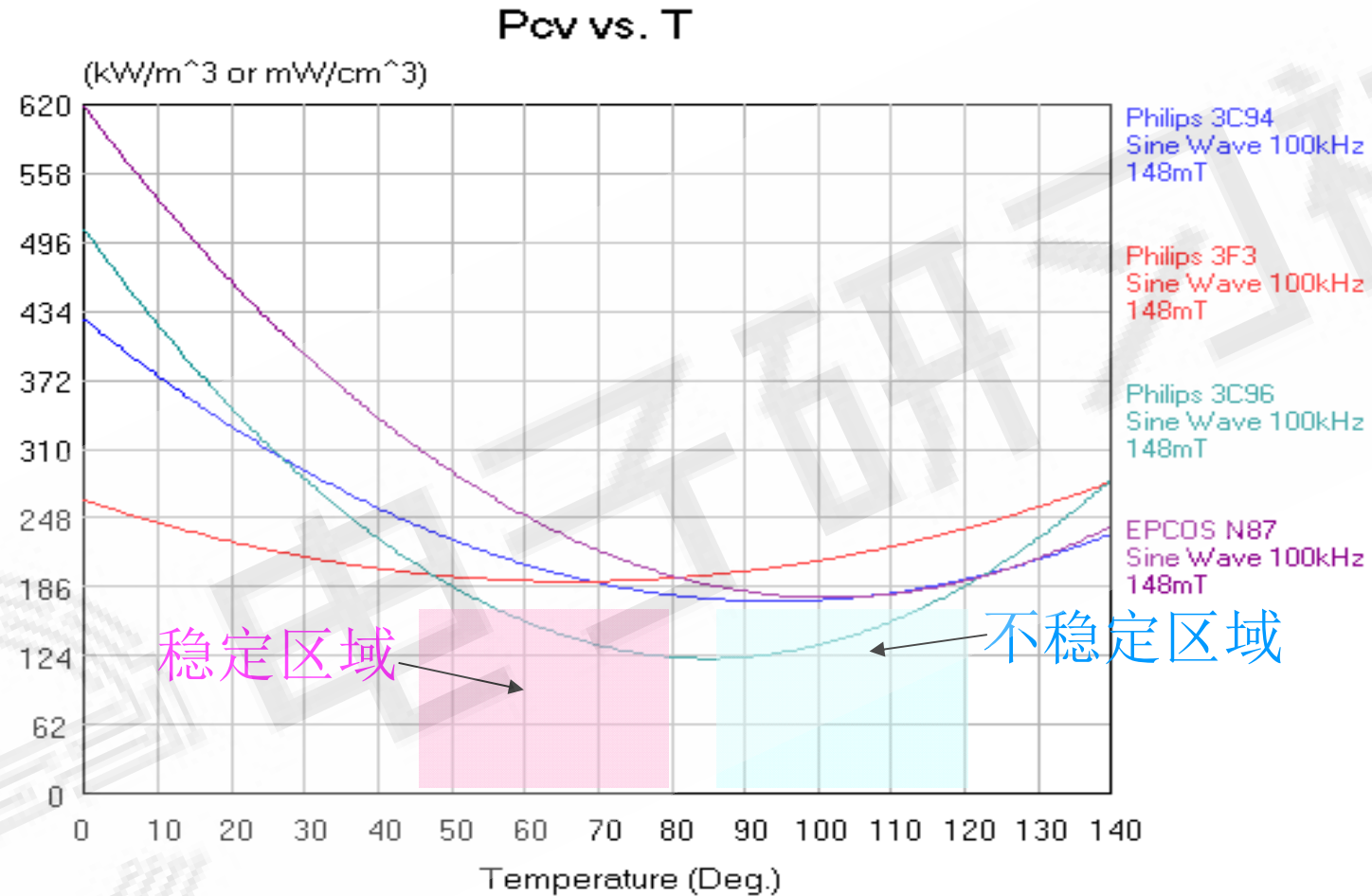
目前高频磁芯材料滞后开关器件的高频化发展及产品需求；
但高频高密度, 但也为磁性元件提出了更高要求和更多机会；
磁芯不仅形状和尺寸需要定制, 而且磁芯材质特性也需要定制化。



- 磁芯损耗与如下因素有关：
- 材料材质；
 - 工作频率 f ；
 - 交流磁密 B_{ac} ；
 - 工作温度 T ；
 - 直流偏磁磁密 B_{dc} ；
 - 励磁波形 D 。



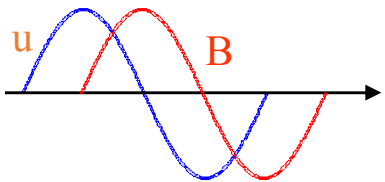
$$P_{CV} = K \cdot f_s^\alpha \cdot B^\beta \cdot (C_0 + C_1 \cdot T + C_2 \cdot T^2)$$



- 温度对铁氧体磁芯损耗有很大影响
- 磁芯温度设计点是很重要的



PWM波形激励下的磁芯损耗



加权平均变化率: \bar{B}_w

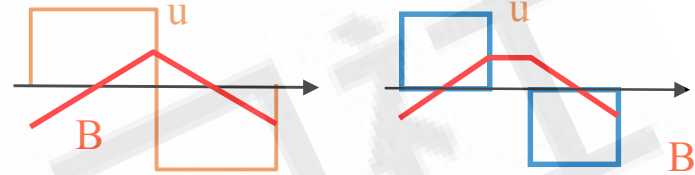
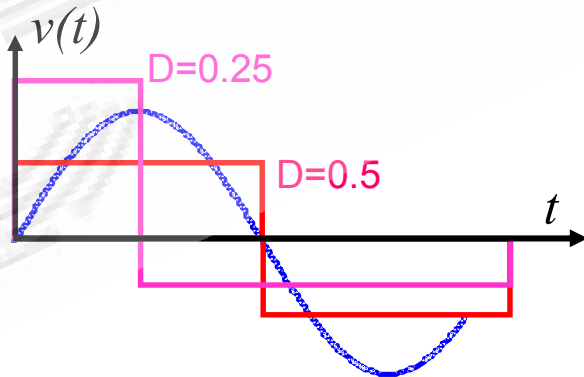
$$\bar{B}_w = \frac{1}{B_{\max} - B_{\min}} \int_T \left(\frac{dB}{dt}\right)^2 dt$$

$$\bar{B}_{w_sin} = (B_{\max} - B_{\min}) \cdot \frac{\pi^2}{2} \cdot f_{sin_eq}$$



$$f_{sin_eq} = \frac{2}{\pi^2} \sum_k \left(\frac{B_{k+1} - B_k}{B_{\max} - B_{\min}}\right)^2 \cdot \frac{1}{t_{k+1} - t_k}$$

Or, $f_{sin} = \frac{2}{\pi^2} \cdot \frac{4}{\left(\int_T |v(t)| dt\right)^2} \int_T v(t)^2 dt$



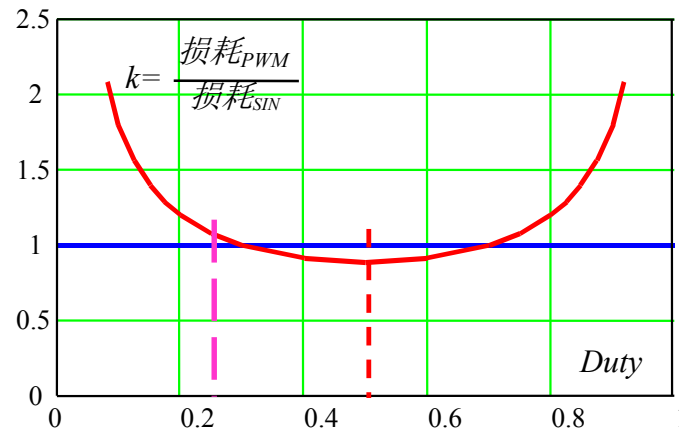
$$\bar{B}_{w_arb} = \frac{1}{(B_{\max} - B_{\min})} \sum_k \frac{(B_{k+1} - B_k)^2}{t_{k+1} - t_k}$$

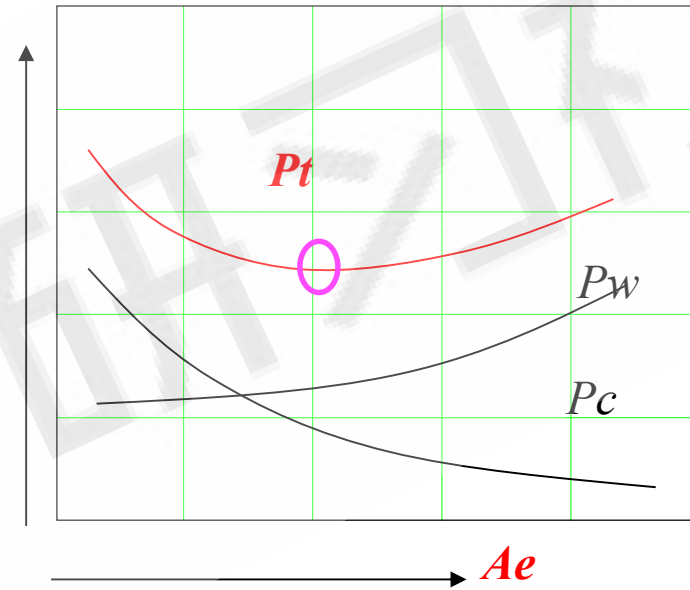
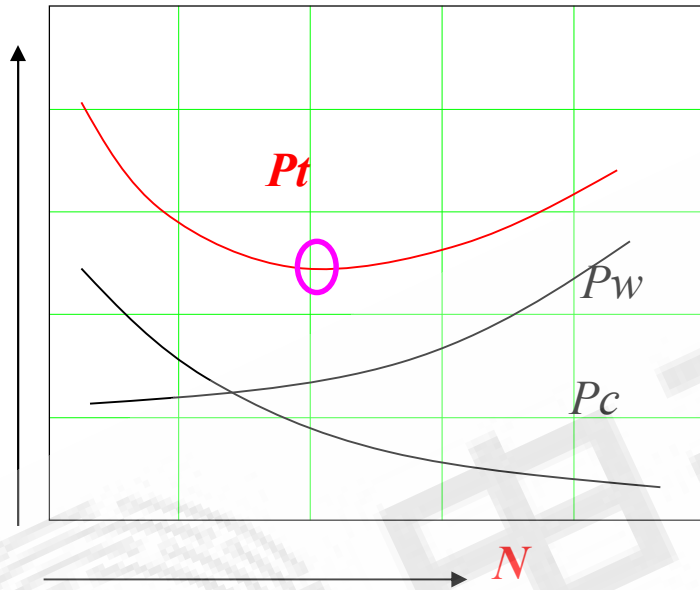
$$P_{cv} = K \cdot f_s^\alpha \cdot B_{ac}^\beta$$

$$P_{cv} = f_s \cdot (K \cdot f_s^{\alpha-1} \cdot B_{ac}^\beta) \quad \text{SIN 励磁}$$

$$P_{cv} = f_s \cdot (K \cdot f_{sin_eq}^{\alpha-1} \cdot B_{ac}^\beta) \quad \text{PWM 励磁}$$

Power loss factor, k, with same Bm and fs





□ 设计合适的绕组匝数和磁芯面积以优化磁件总损耗

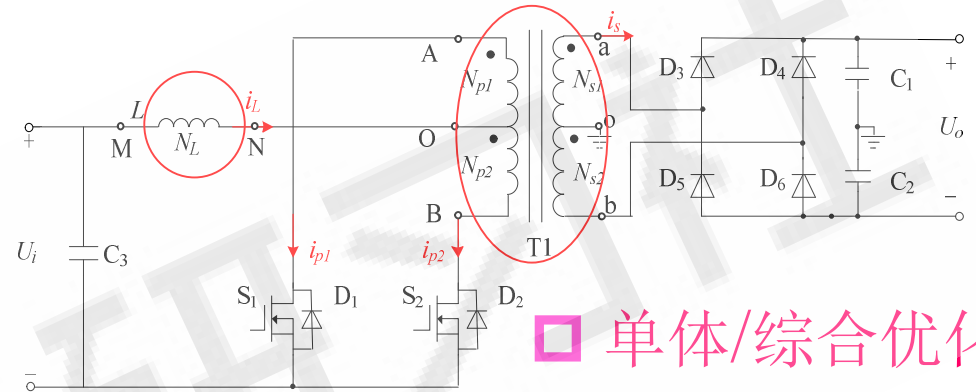
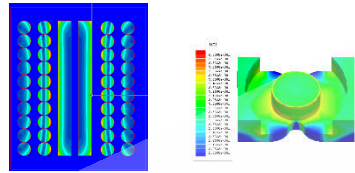
1、损耗模型

理论模型

$$J_y(x) = k \cdot \frac{H_1 \cosh[k(d-x)] - H_2 \cosh(kx)}{\sinh(kd)}$$

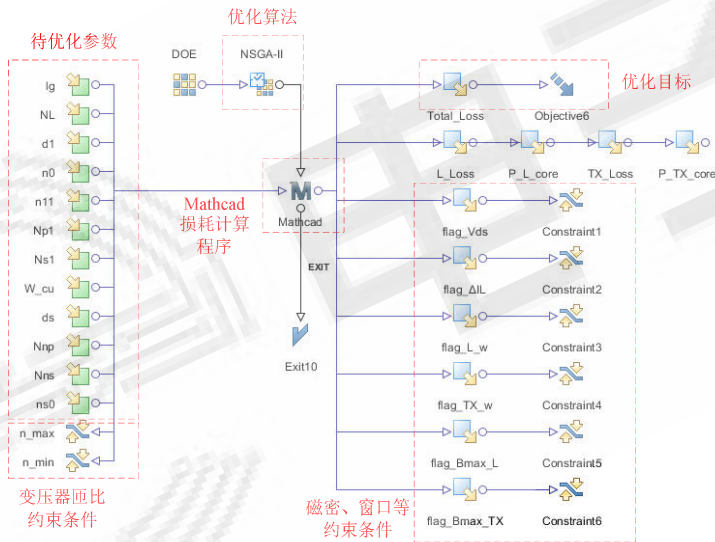
$$P_{cv_dc} = P_{cv_ac} \cdot \frac{1 + \kappa_1 \cdot B_m^{-\delta_1} \cdot \left(\frac{H_{dc}}{\kappa_2 \cdot B_m^{-\delta_2}}\right)^\beta}{1 + \left(\frac{H_{dc}}{\kappa_2 \cdot B_m^{-\delta_2}}\right)^\beta}$$

仿真模型

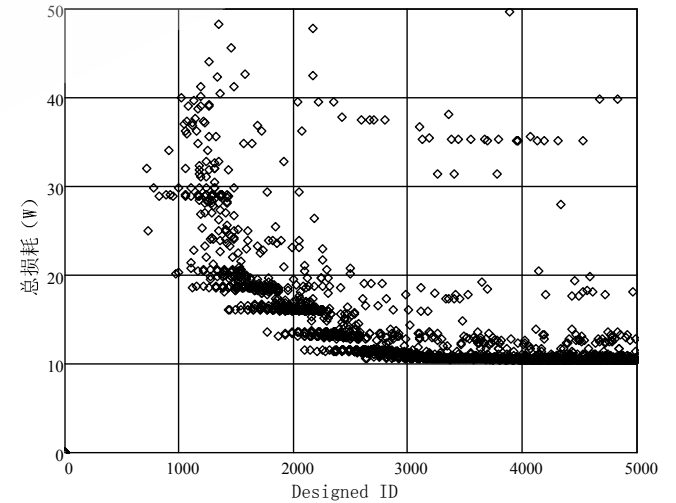


□ 单体/综合优化

2、优化算法

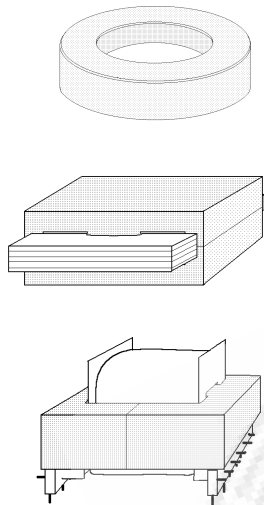


3、优化过程



- 损耗模型的准确有效与实用最为关键
- 绕组损耗/线规优化 → 单磁元件磁芯、绕组组合优化 → 多磁元件综合优化

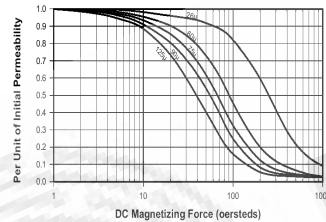
结构设计



空间可行性

电气设计

$$L = \frac{\mu \cdot N^2 A_e}{l_e}$$



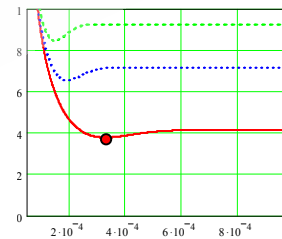
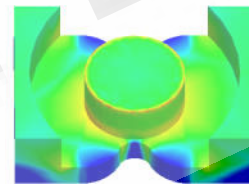
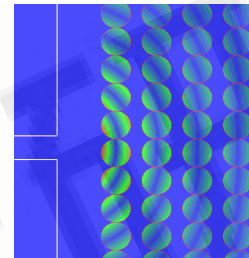
电气可行性

杂散参数



电应力

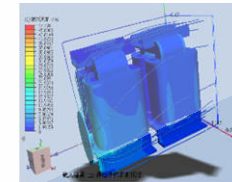
损耗设计



效率/功率密度

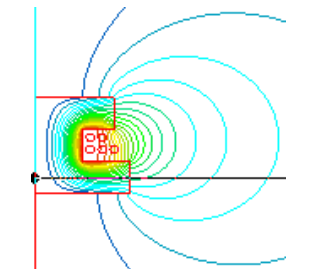
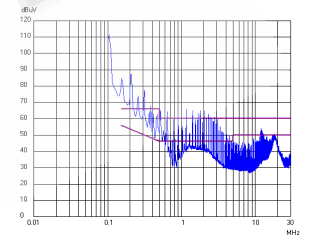
热设计

$$\Delta T = \left(\frac{P}{S}\right)^{0.833}$$

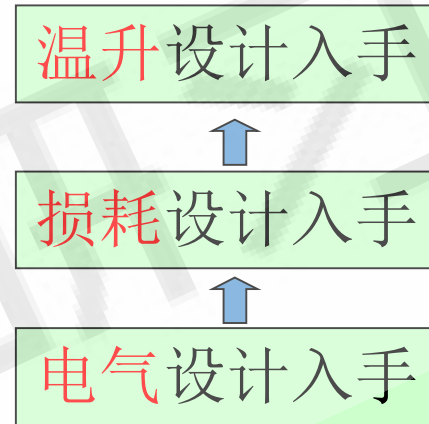
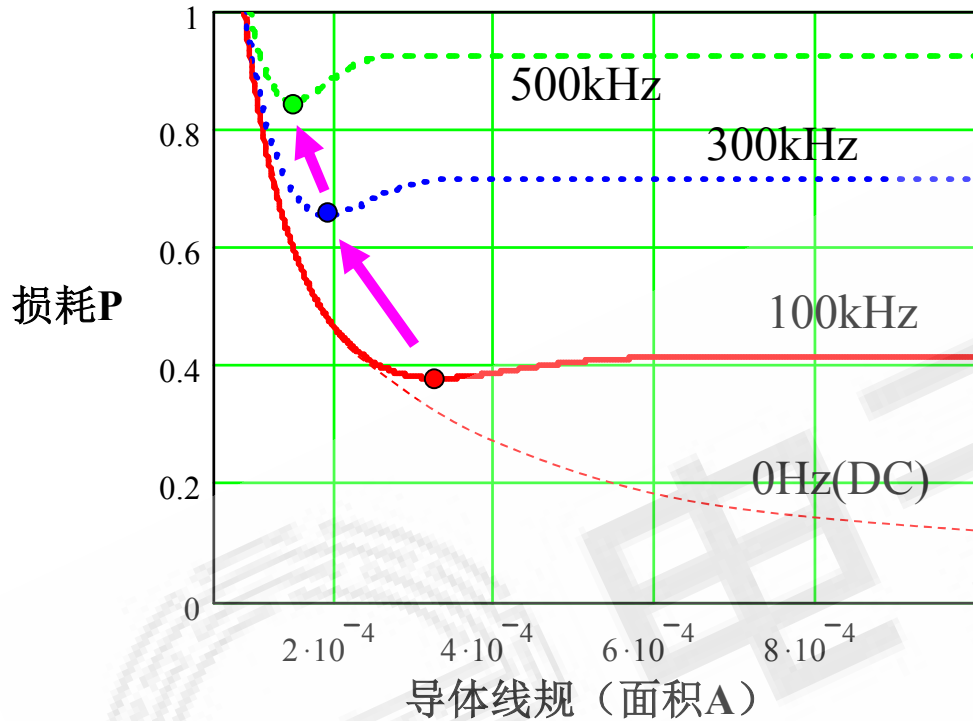


温升规范

EMI设计

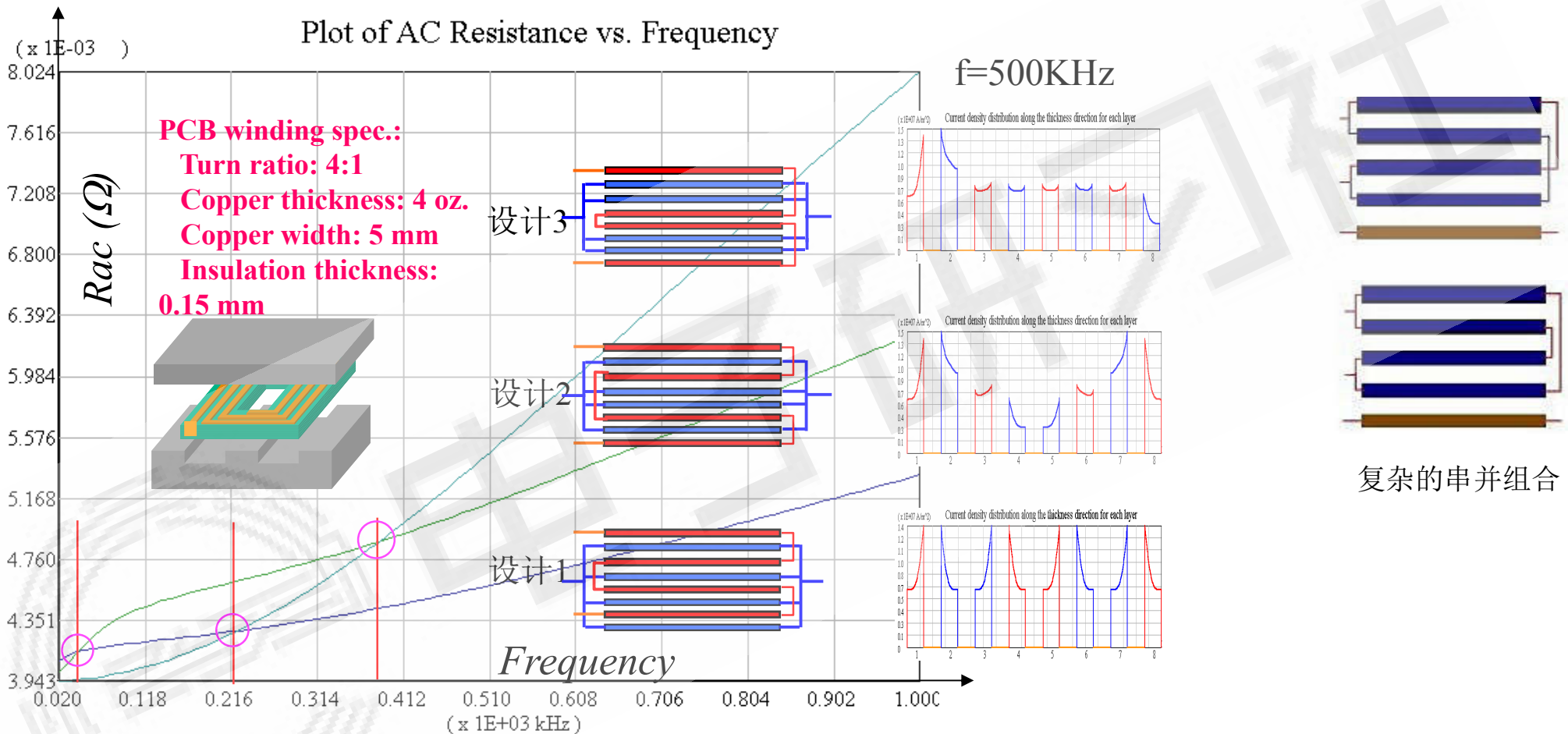


EMC规范



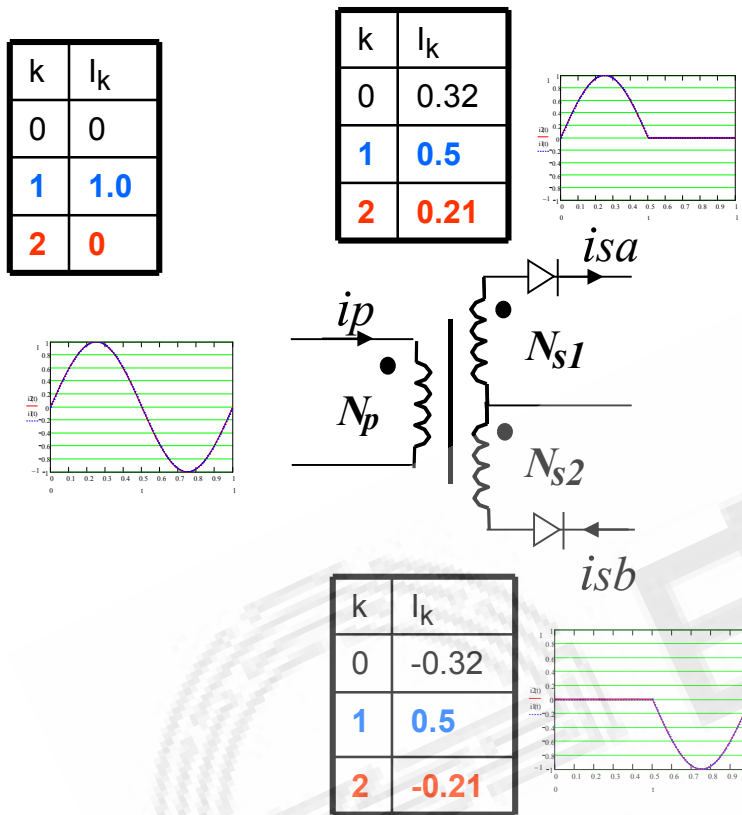
↑ 频率提高

- 频率提高，最优导体面积减小，但损耗增加，损耗密度(温升)显著增大
- 使得磁性元件的设计向着从损耗设计和温升设计入手发展。

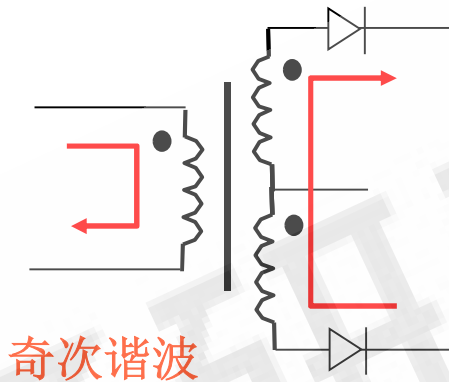


□ 多层PCB绕组设计十分灵活，但排布及连接方案（串、并组合）众多，且需要综合考虑损耗、漏感以及分布电容。

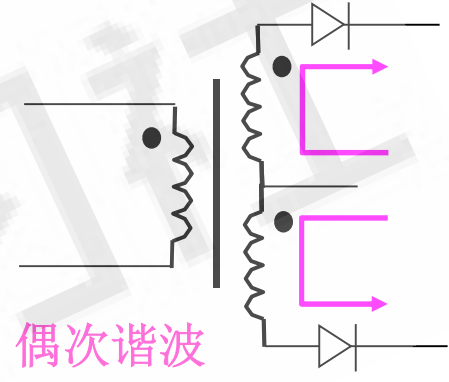
LLC变压器电流谐波与绕组结构



频域安匝平衡

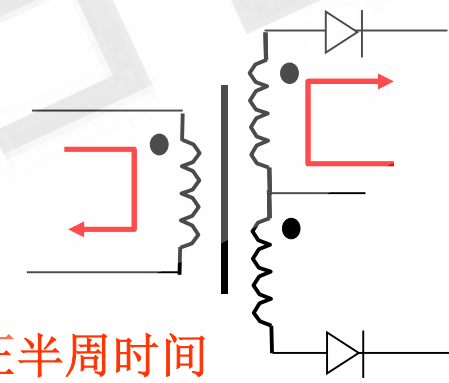


奇次谐波

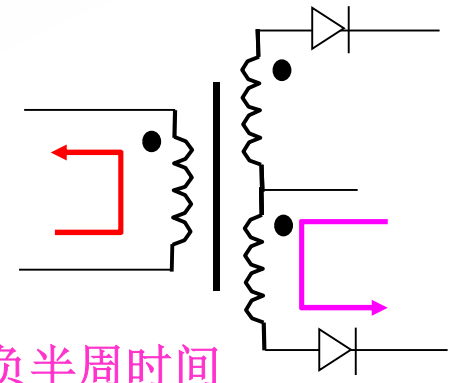


偶次谐波

时域安匝平衡



正半周时间

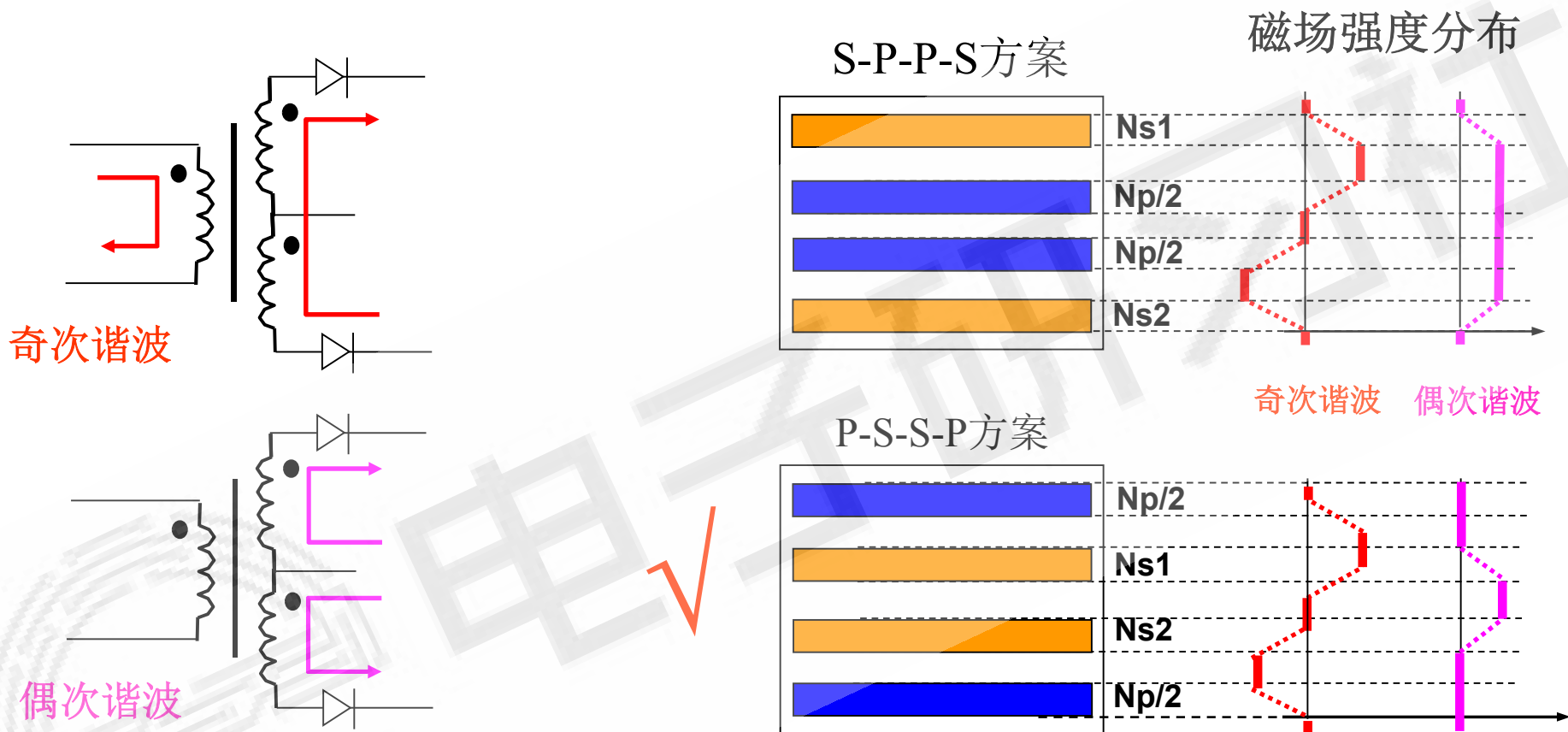


负半周时间

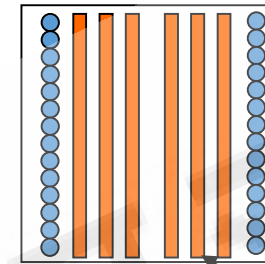
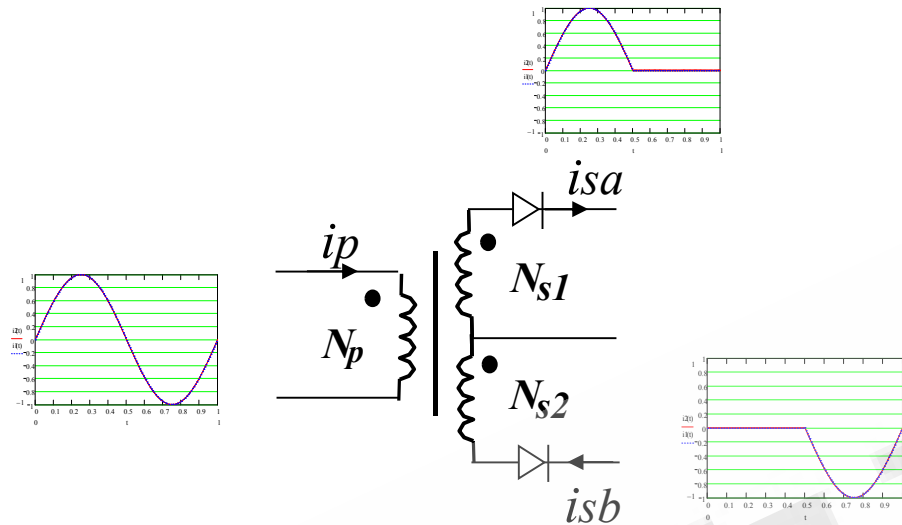
- 奇次MMF在原边(N_p)与两个副边($N_{sa}+N_{sb}$)间平衡
- 偶次MMF只在副边两绕组间平衡 (N_{sa} and N_{sb})



LLC变压器电流谐波与绕组结构



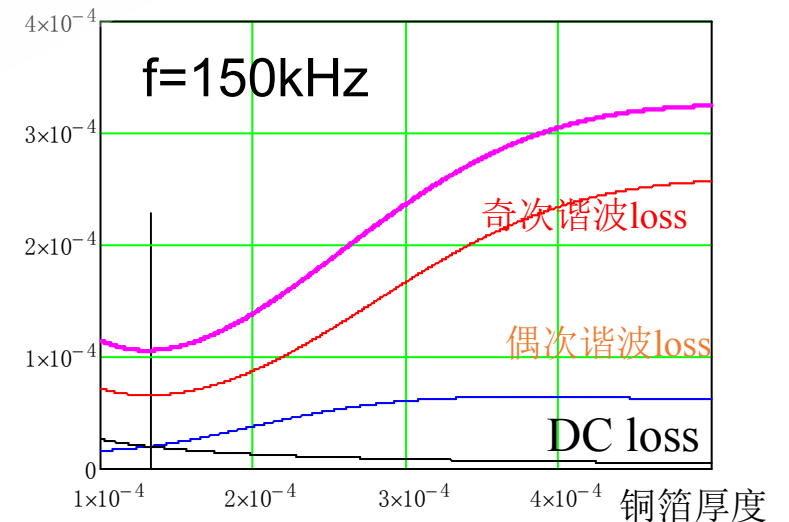
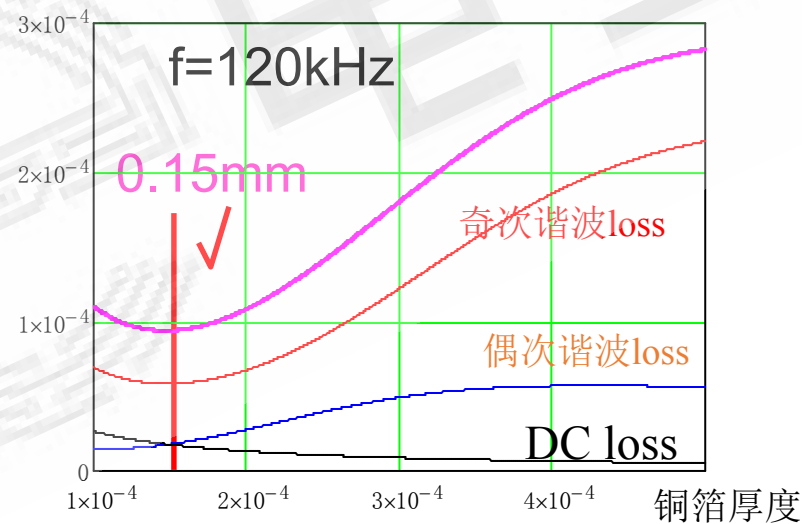
对于副边抽头全波整流，P-S-S-P为最佳绕组结构



$N_p:N_{s1}:N_{s2}=15:3:3$

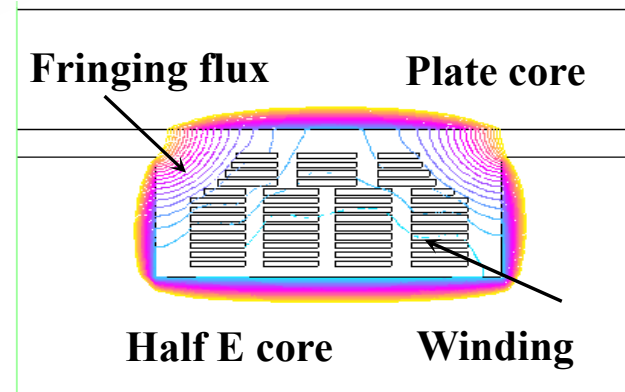
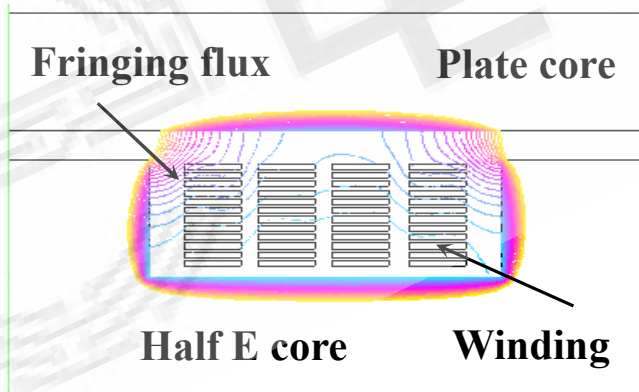
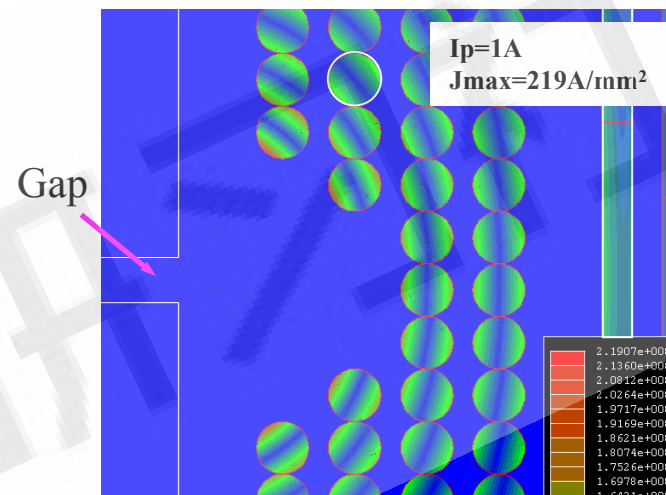
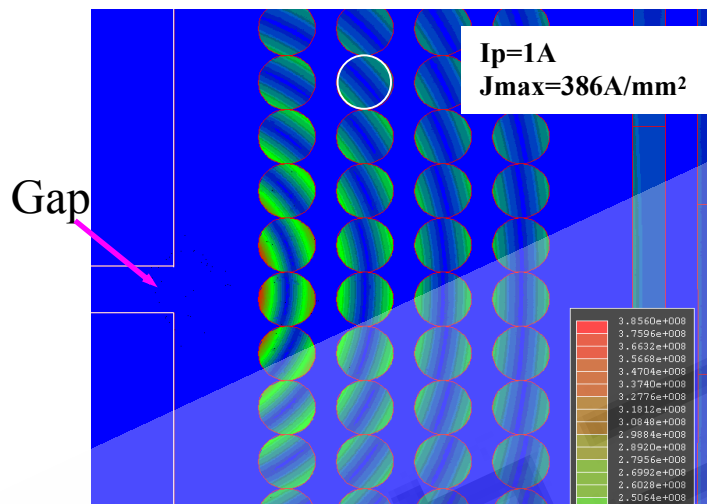
3T
3T

CU PLATE (0.15X22)mm ✓
CU PLATE (0.15X22)mm



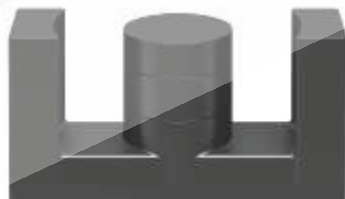
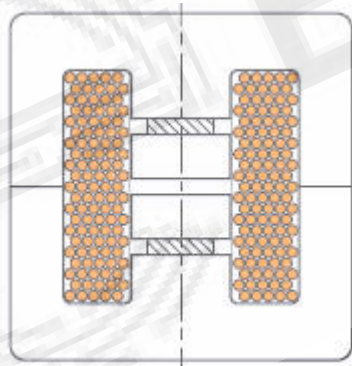
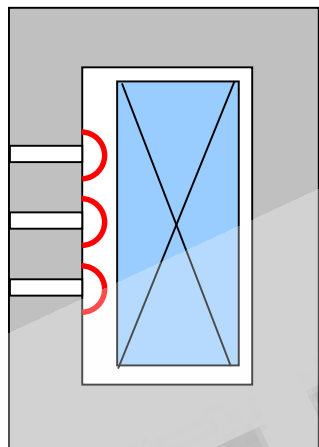
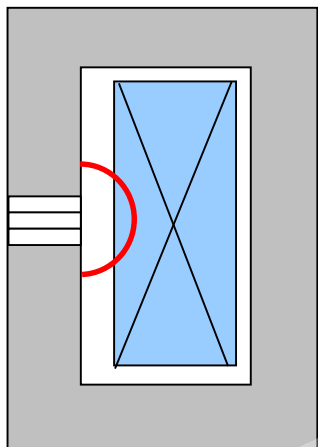


降低气隙扩散磁通损耗—气隙避让





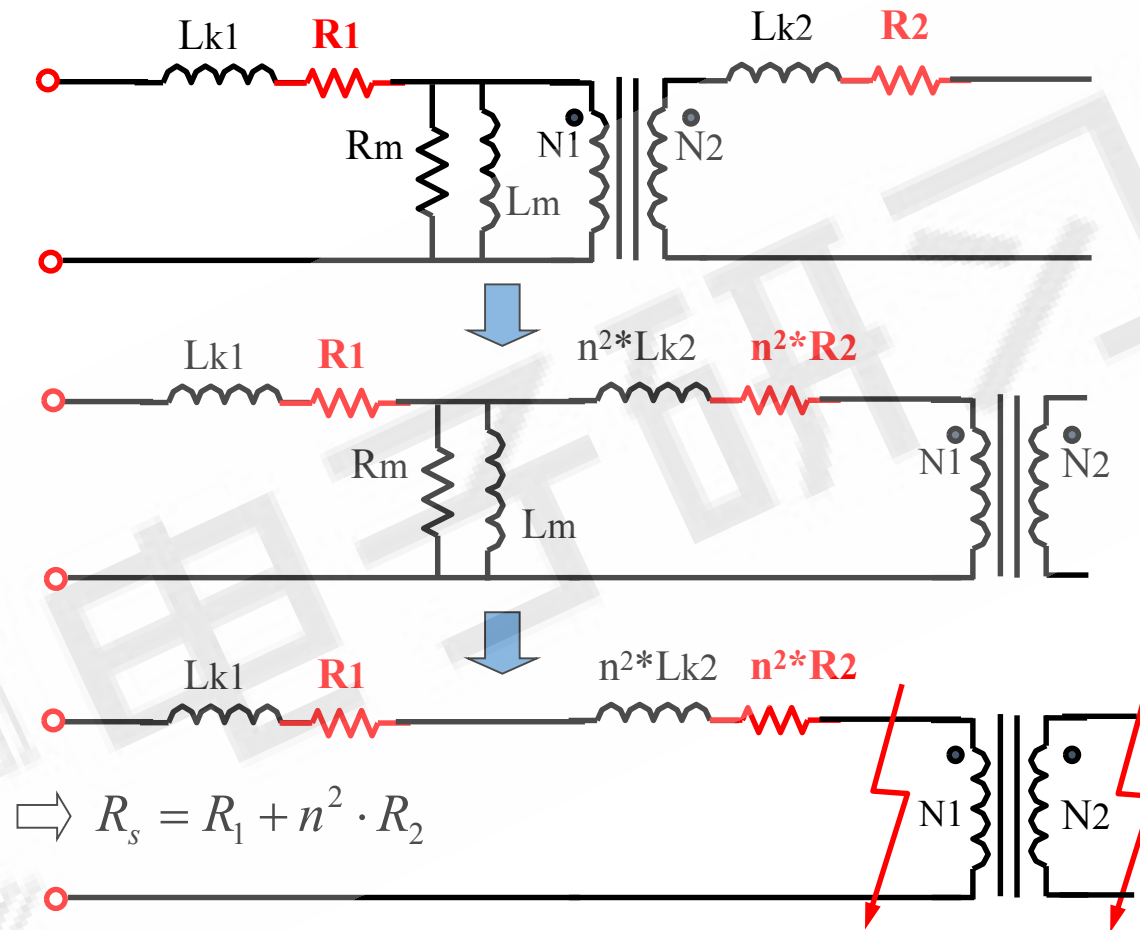
降低气隙扩散磁通损耗—分布气隙



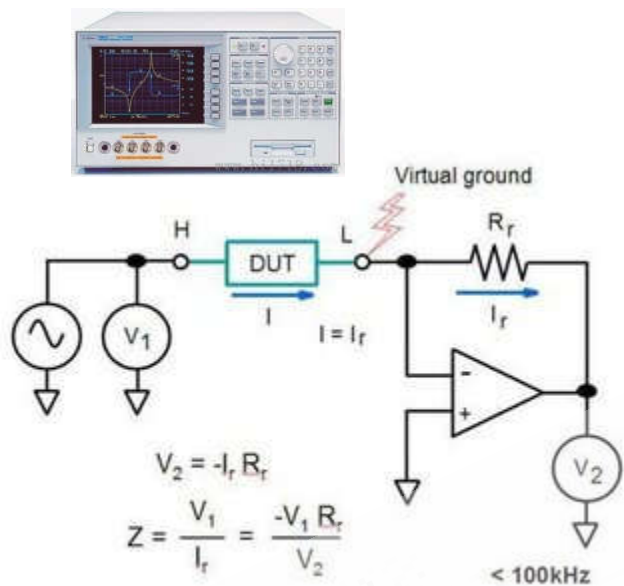
Benefits

- Significantly increased power density
- Up to 70% reduction in leakage field losses
- Enables use of a larger winding area by reducing fringing flux
- Low winding losses compared to a single large air gap
- Reduction of core size by one class thanks to lower winding losses, e.g. E 65 → E 55 or ETD 59 → ETD 54
- Enables copper saving

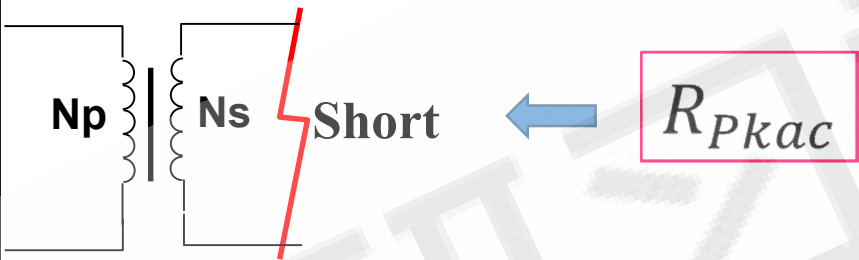
TDK: Distributed Air Gaps in Ferrite Cores



- 由于线圈交流损耗是线性的，因此可以通过阻抗分析仪测量
- 由于线圈副边短路，磁芯没有磁通和损耗，因此只有绕组损耗
- 对于变压器，原边绕组和副边绕组的损耗是难以分离的



阻抗分析仪



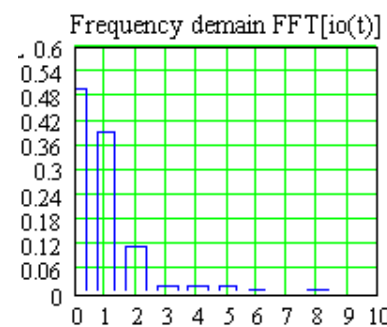
R_{kac} : 第k次谐波对应的交流电阻

I_k : 第k次电流谐波有效值

I_{Pkac}



$i(t)$ waveform



Harmonics

$$P_W = I_{dc}^2 \cdot R_{dc} + \sum_{\text{所有次谐波}k} (I_{Pkac}^2 \cdot R_{Pkac})$$

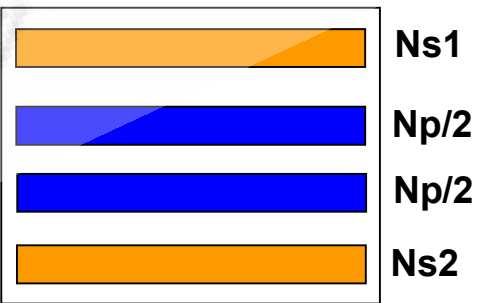


R_{Pkac} 对于 $k=$ 奇次

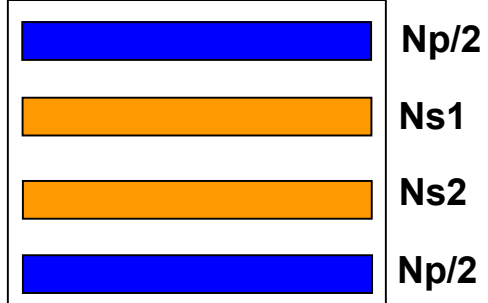
R_{Skac} 对于 $k=$ 偶次

$$P_W = I_{dc}^2 \cdot R_{dc} + \sum_{\text{奇次谐波}k} (I_{Pkac}^2 \cdot R_{Pkac}) + \sum_{\text{偶次谐波}k} (I_{Skac}^2 \cdot R_{Skac})$$

S-P-P-S方案



P-S-S-P方案





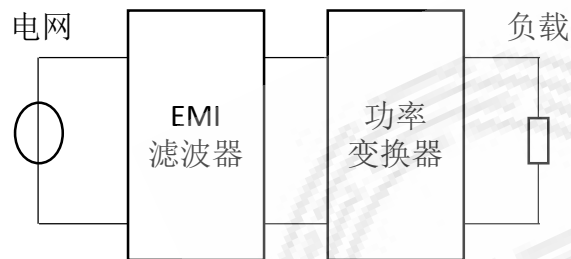
车载充电机

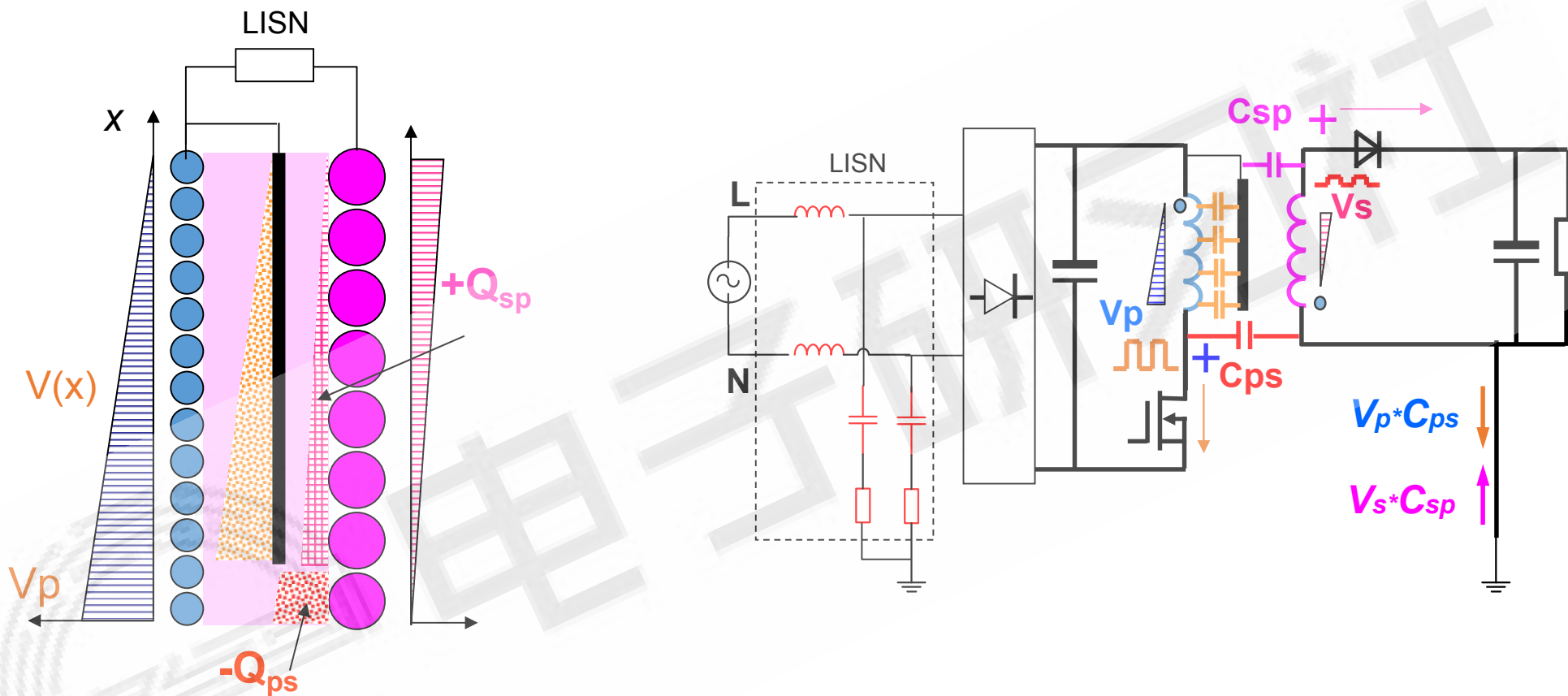
功率变换器:

- 选择合适电路拓扑
 - ★ 减少电位跳变点: 如改进无桥PFC
 - ★ 减小I/O电流纹波: 如多路交错, 磁集成
- 减缓开关波形速率
 - ★ 减缓驱动速度: 如加大驱动电阻
 - ★ 减小开关冲击: 局部谐振软开关
 - ★ 减小振荡毛刺: 如管脚套磁珠, 并电容
- 降低开关电压峰值
 - ★ 增加RCD/RC吸收电路
- PCB布板
 - ★ 减小高频回路长度/面积
 - ★ 避免布线干扰耦合
- 电磁屏蔽
 - ★ 机壳电磁屏蔽
 - ★ 元件电磁屏蔽
- 磁性元件 (电感器、变压器)

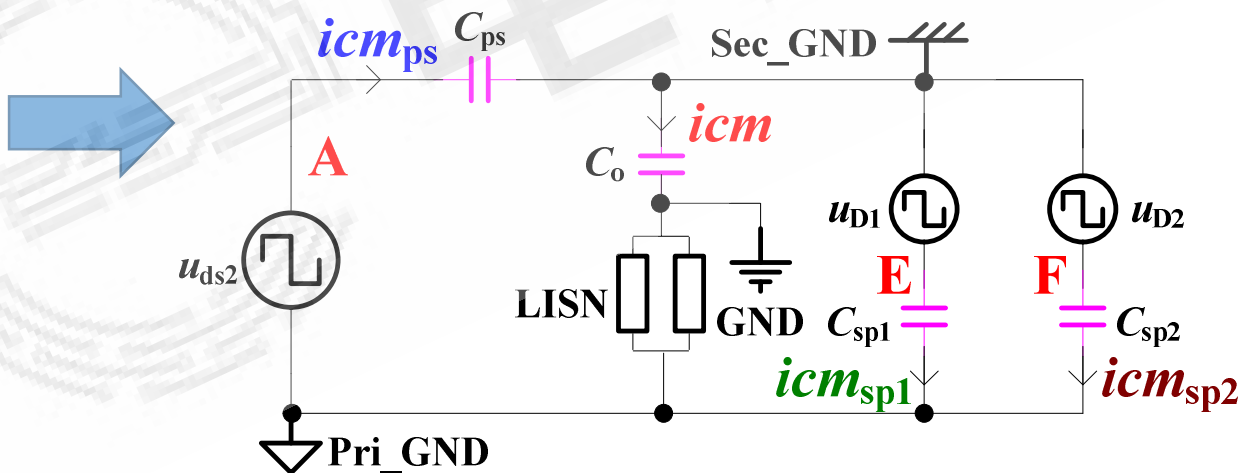
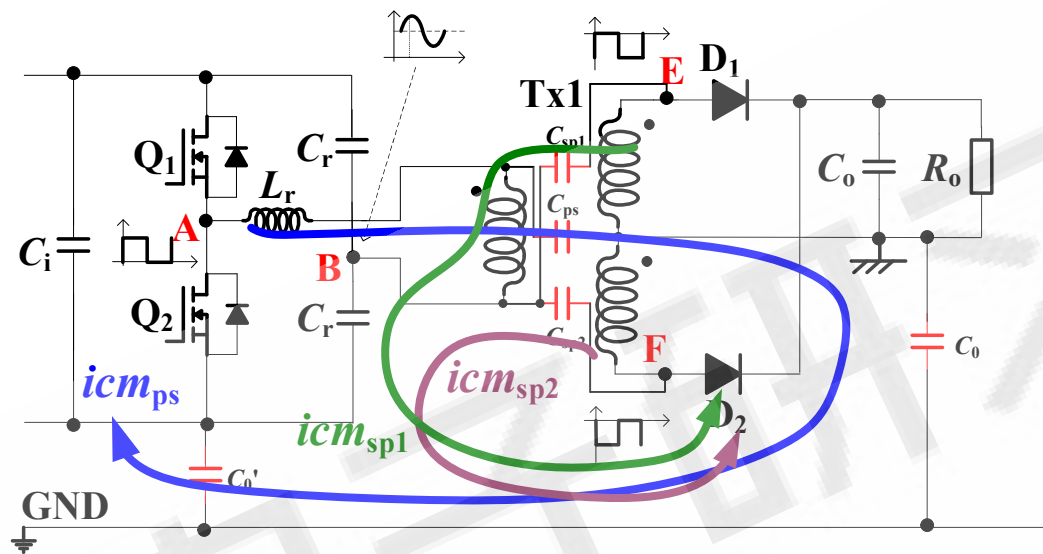
滤波器:

- 拓扑结构
 - ★ 增加滤波器级数
- 元件参数
 - ★ 增加电容、电感量
- 滤波电感
- 滤波元件电磁耦合



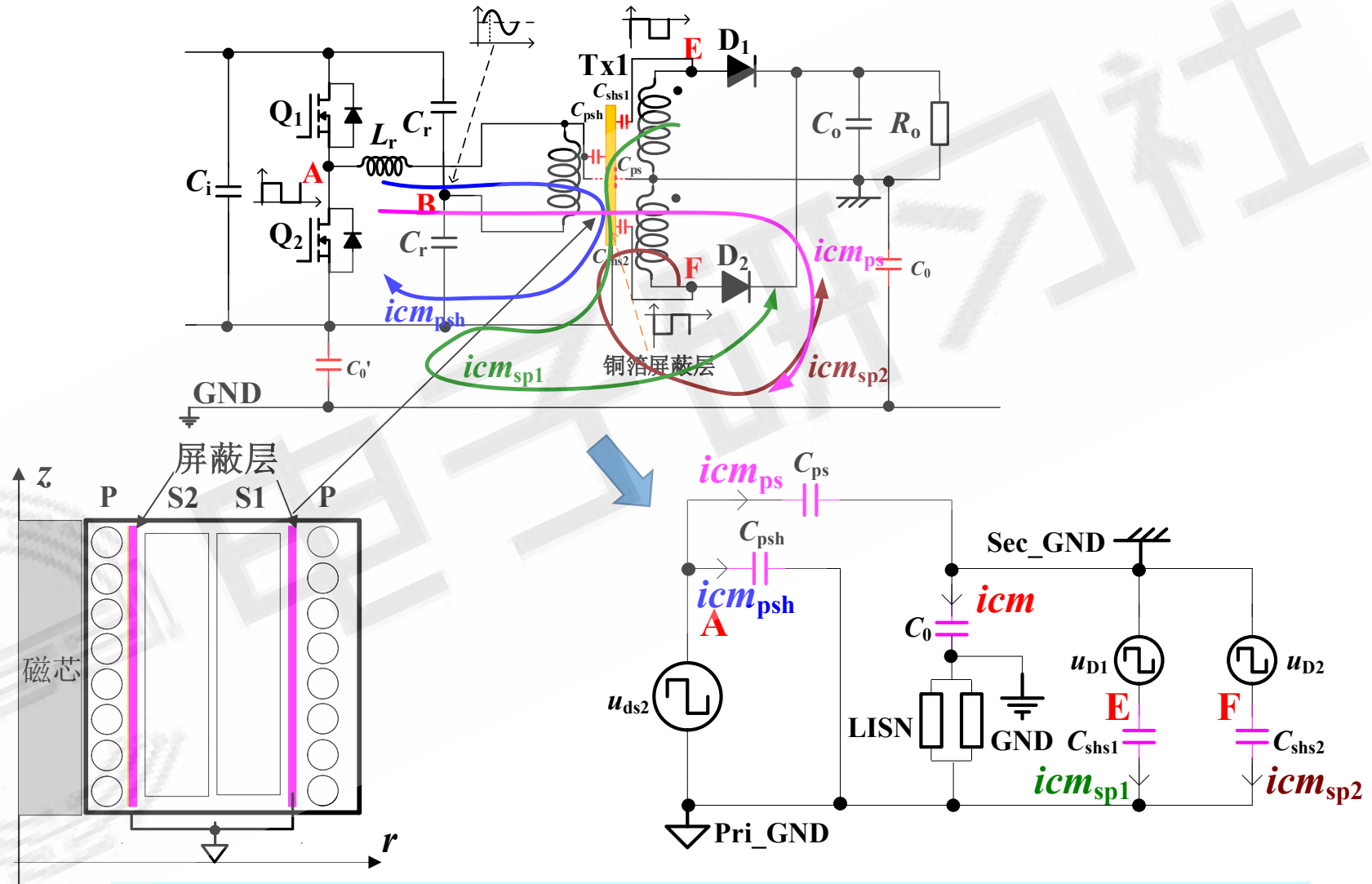


□ 当 $Q_{ps} = Q_{sp}$ ，即当 $V_p \cdot C_{ps} = V_s \cdot C_{sp}$ 时，变压器副边的净电荷将相互抵消为零，

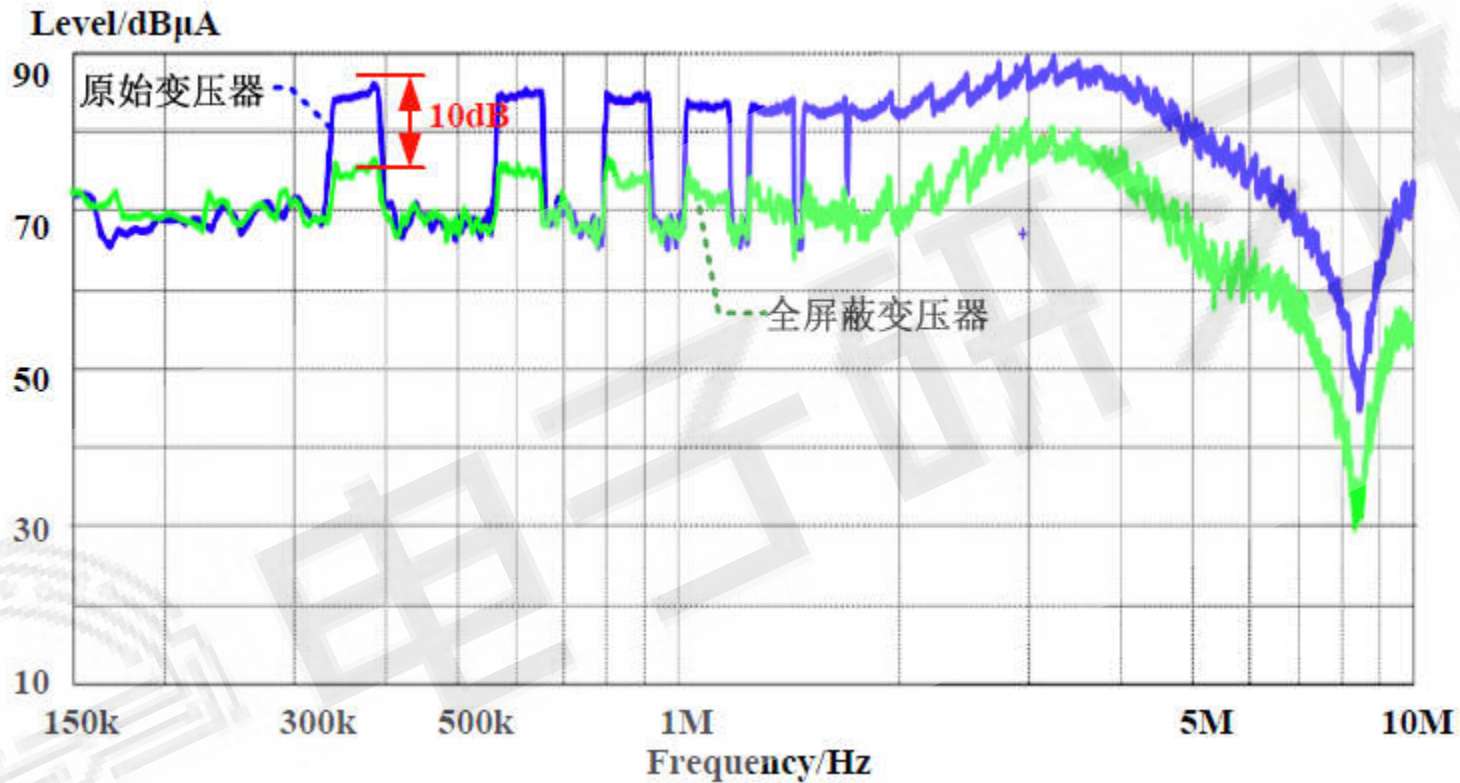


u_{D1} , u_{D2} 幅值相等、相位相反，产生的共模噪声电流 $i_{cm_{sp1}}$ 和 $i_{cm_{sp2}}$ 相位相反。

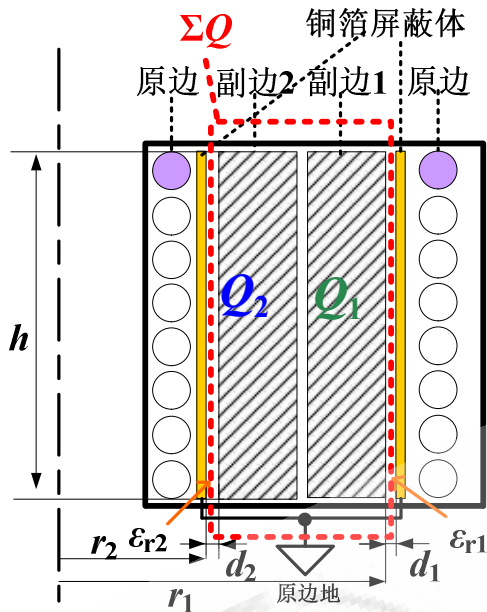
LLC电路副边噪声源影响噪声抵消考虑



- 原副边加屏蔽层可减小噪声;
- 如果 $C_{sp1} = C_{sp2}$, 则副边电位变化引起的共模噪声抵消;



- 采用全屏蔽变压器相比于原始变压器在整个频段内均有改善且在150kHz~2MHz 范围内改善了10dB 左右



$Q=C*U$
电压分布对称

$$r_1 > r_2$$

$$|Q_1| > |Q_2|$$

$$C_0 = \epsilon_0 \cdot \epsilon_r \cdot \frac{A}{d}$$

A : 两极板正对面积;

d : 两极管间的距离;

ϵ_r : 两极板间介质的介电系数。

LLC变压器两副边与屏蔽体间的结构电容比较:

由: $\epsilon_{r1} = \epsilon_{r2}$, $d_1 = d_2$, $r_1 > r_2$

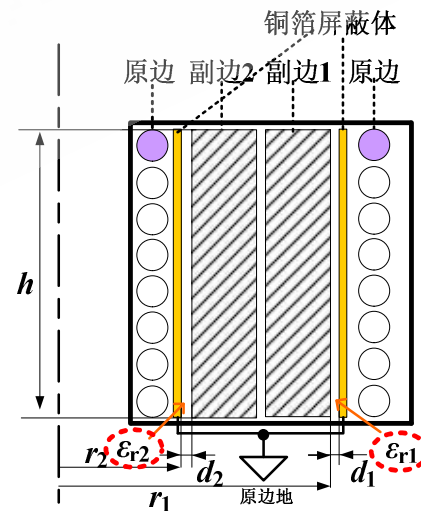
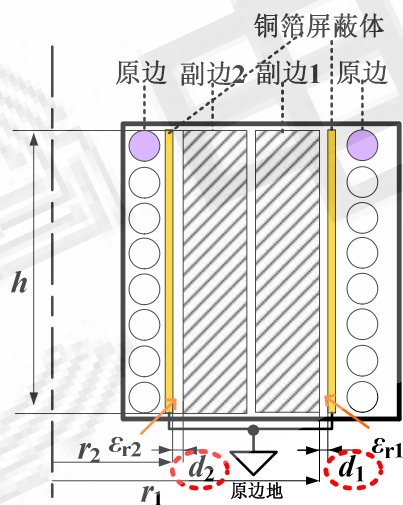
则:

$$C_{01} = \frac{\epsilon_0 \cdot \epsilon_{r1} \cdot 2\pi \cdot r_1}{d_1} > C_{02} = \frac{\epsilon_0 \cdot \epsilon_{r2} \cdot 2\pi \cdot r_2}{d_2}$$

全屏蔽方案中共模噪声是由两副边与屏蔽层的结构电容不对称造成的

优化设计距离和相对介电系数

- 调节两副边与屏蔽层间的距离，使 $d_1/d_2=r_1/r_2$ ，即 $C_{01}=C_{02}$ ；
- 调节两副边与屏蔽层间的相对介电常数，使 $\varepsilon_{r1}/\varepsilon_{r2}=r_2/r_1$ ，即 $C_{01}=C_{02}$ ；
- 同时调节 d_1 、 d_2 和 ε_{r1} 、 ε_{r2} ，使 $\frac{d_1 \cdot \varepsilon_{r2}}{d_2 \cdot \varepsilon_{r1}} = \frac{r_1}{r_2}$ ，即 $C_{01}=C_{02}$ ；

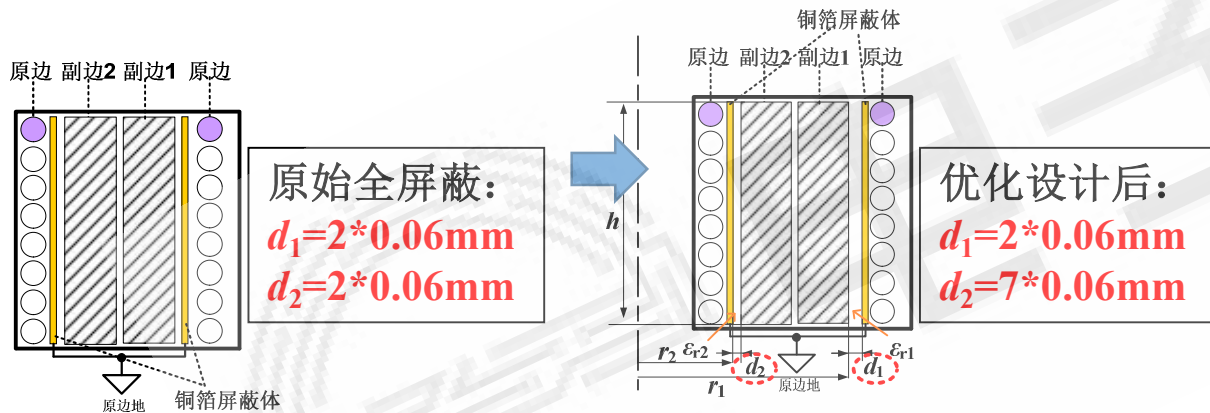


□ 调节距离与相对介电系数可消除LLC变压器的共模噪声

实验验证 (I) - 调节距离

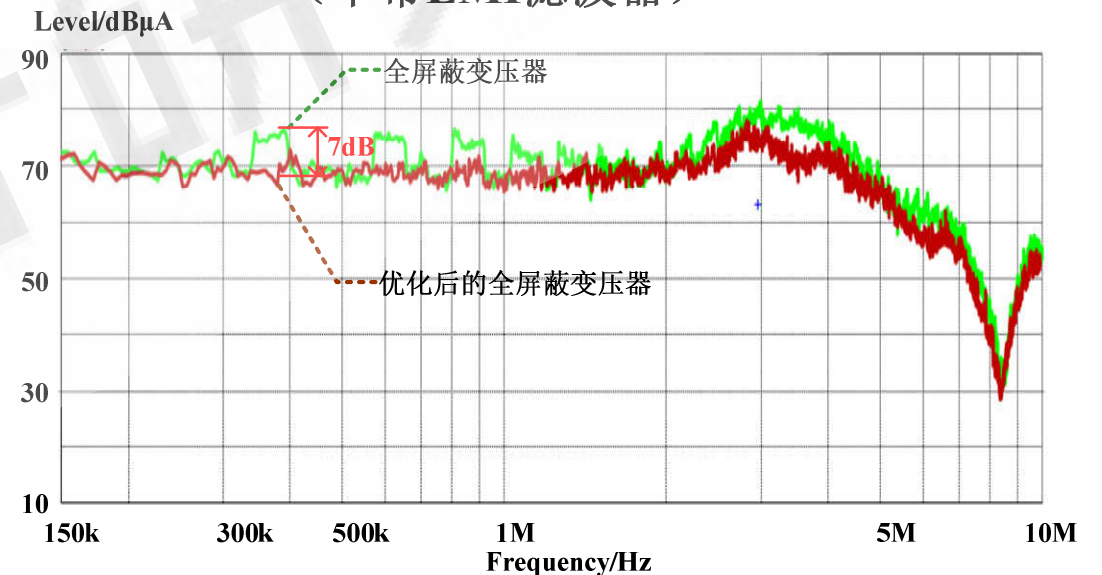
采用调节两副边绕组与屏蔽层间的距离

- ◆ 输入电压：220VAC&50Hz
- ◆ 输出电压：53V&50A
- ◆ PFC开关频率：30kHz~110kHz
- ◆ LLC开关频率：115kHz~135kHz



	变压器Tx1		变压器Tx2	
	C_{shs1} (pF)	C_{shs2} (pF)	C_{shs1} (pF)	C_{shs2} (pF)
优化前	100	150	107	157
优化后	110	112	110	115.4

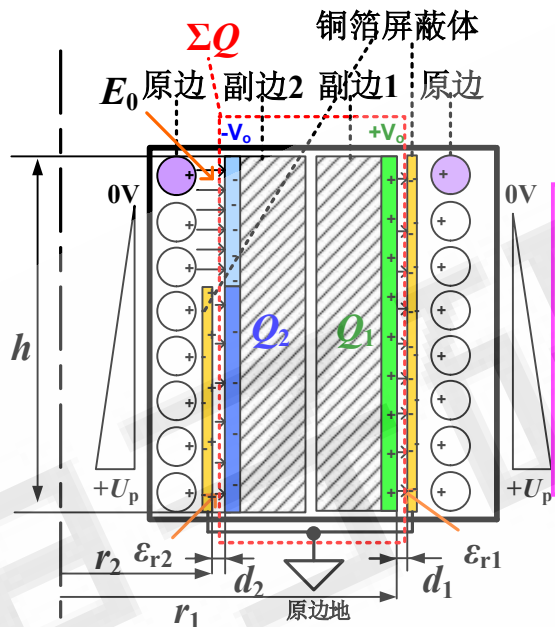
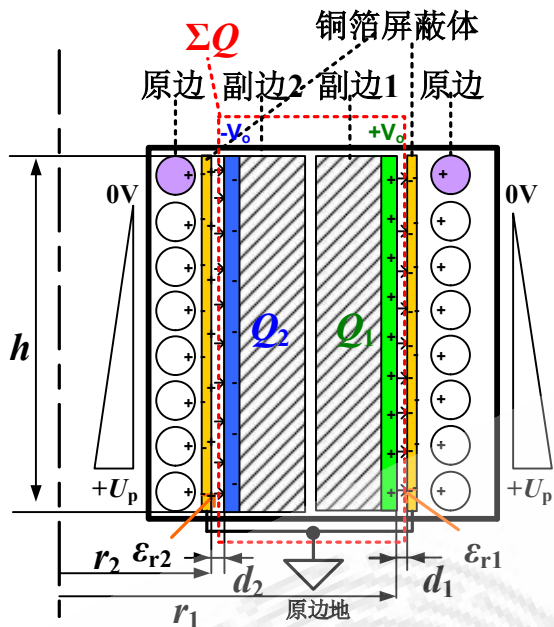
传导共模噪声测试实验结果：
(不带EMI滤波器)



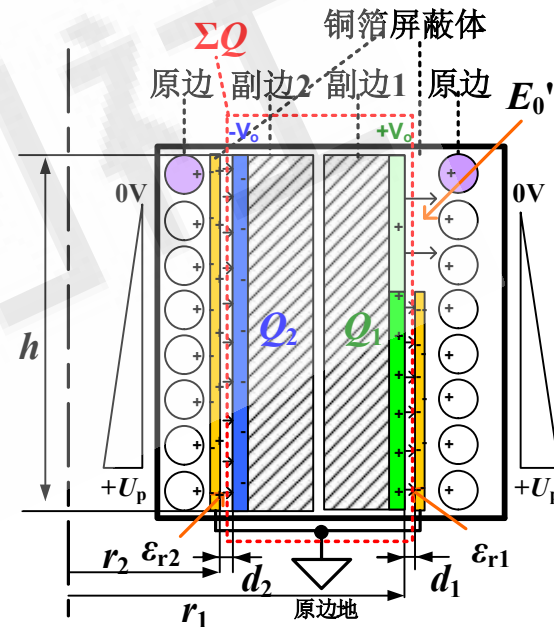
- 全频段内均有改善，在150kHz~1MHz内改善了约7dB;

□ 调节相对距离的实验结果验证了分析的正确性和有效性 42

LLC电路副边噪声优化II



屏蔽层接原边电位静点

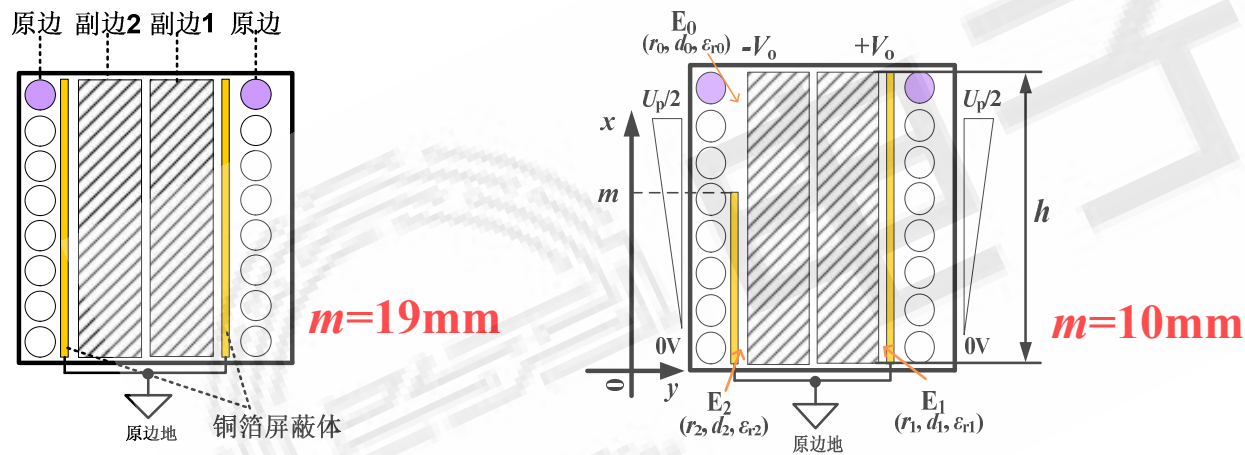


- $|Q_1| > |Q_2|$
- 欲使 $|Q_1| = |Q_2|$, $\Sigma Q = 0$ 则可通过增大 Q_2 或减小 Q_1 。

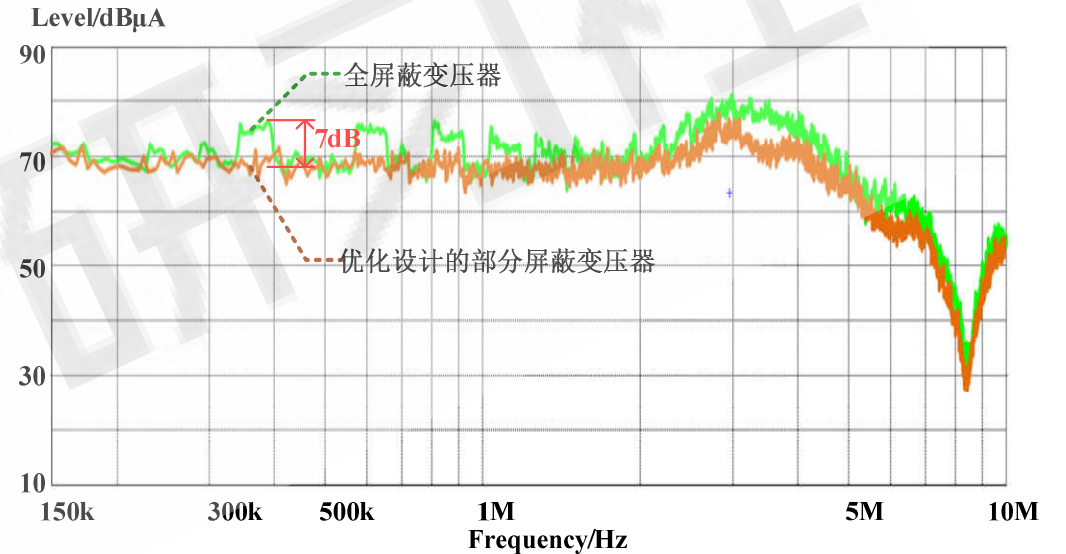
□ 调节屏蔽层的面积可消除LLC变压器的共模噪声

实验验证(II)-调节面积 采用部分屏蔽技术

- ◆ 输入电压: 220VAC&50Hz
- ◆ 输出电压: 53V&50A
- ◆ PFC开关频率: 30kHz~110kHz
- ◆ LLC开关频率: 115kHz~135kHz



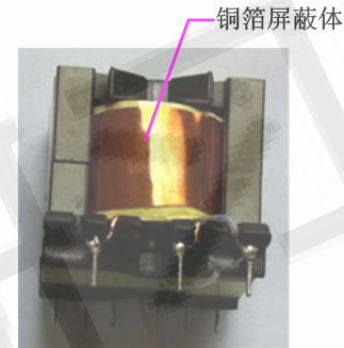
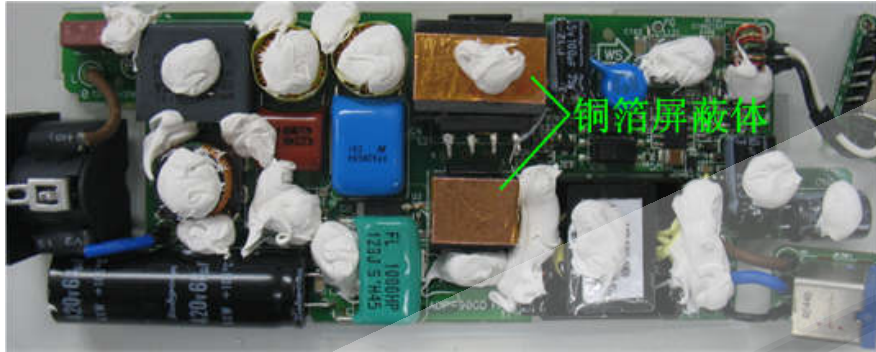
传导共模噪声测试实验结果:
(不带EMI滤波器)



- 全频段内均有改善, 在150kHz~1MHz内改善了约7dB;

□ 部分屏蔽的实验结果验证了分析的分析的正确性和有效性

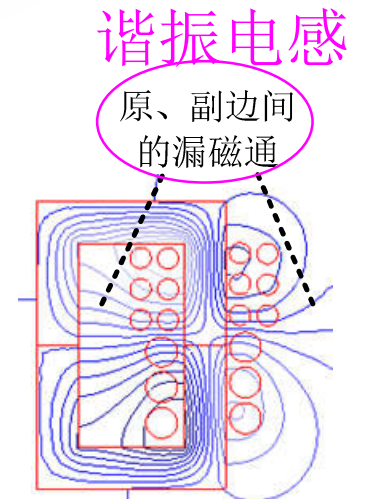
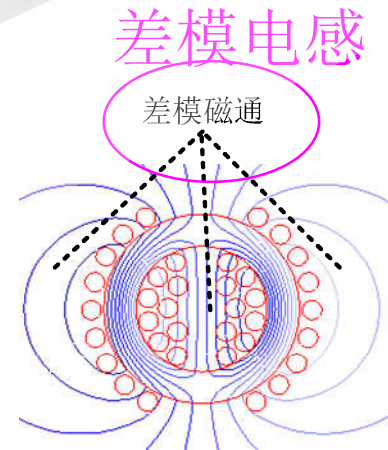
磁性元件由于体积大，其对地电场耦合较大。—传统解决方案：法拉第电磁屏蔽技术



✓ 优点：屏蔽电场

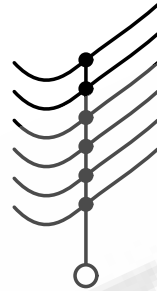
✓ 缺点：

- ① 屏蔽高频磁场，改变磁件磁性参数；
- ② 由于涡流效应所产生的损耗较大。



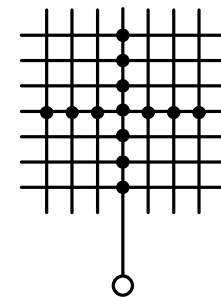
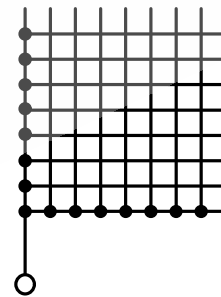
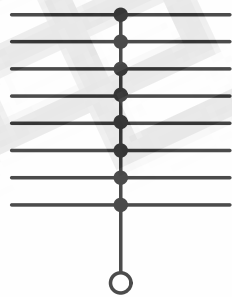
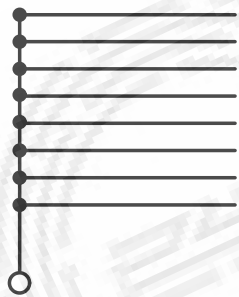
❑ 传统电磁屏蔽体会影响磁件的磁性参数，不适用于一些磁性参数有特殊用途的场合

梳状电场屏蔽体的原理结构：



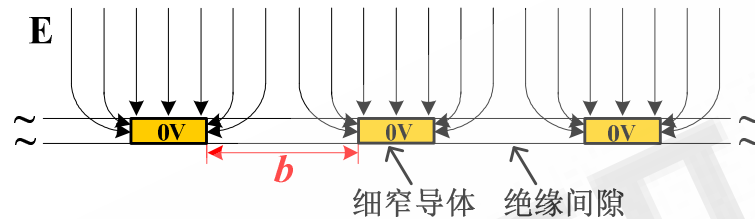
✓ 由若干根细窄金属导线组成梳状或网状；

梳状电场屏蔽体可能的连接结构：

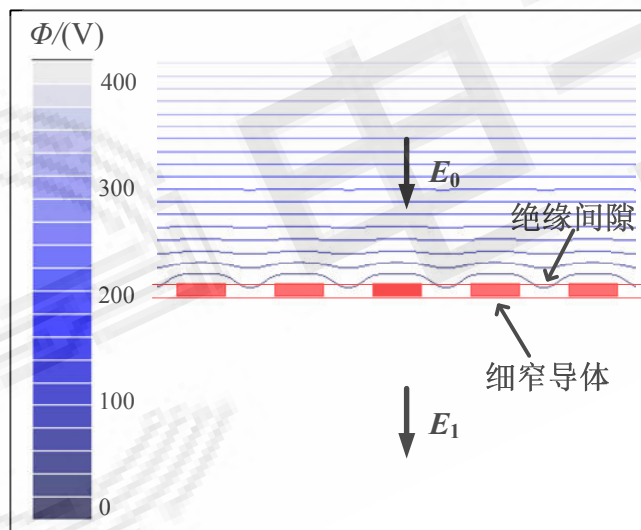


□ 梳状电场屏蔽体由多根细窄导体组成，且不够成电回路

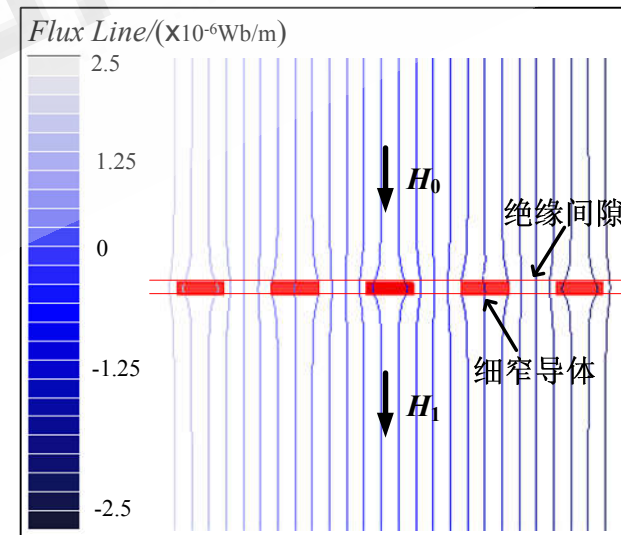
梳状电场屏蔽体电场屏蔽原理：



通过控制两相邻细窄导体间的距离“ b ”来获得所需要的电场屏蔽效果。



屏蔽电场

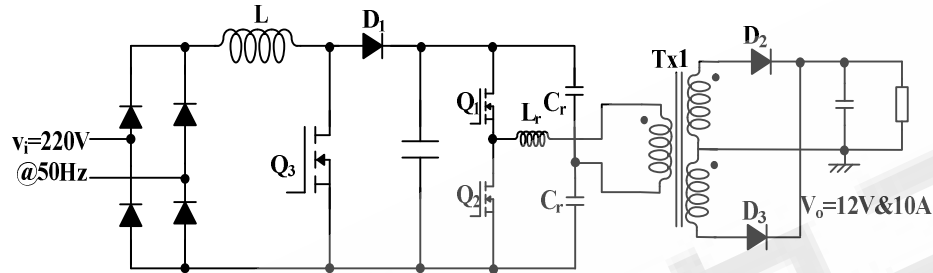


基本不影响高频磁场

□ 梳状电场屏蔽体屏蔽电场、不影响高频磁场

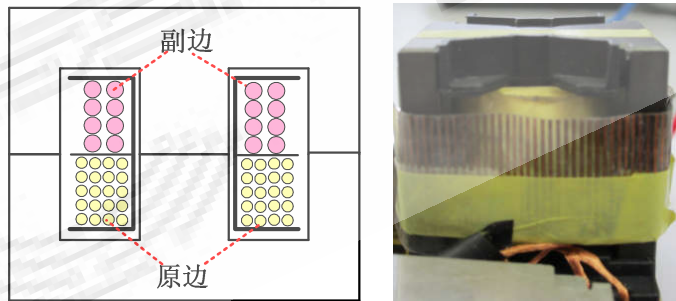
实验样机参数及电路拓扑:

- ◆ 输入电压: 220VAC&50Hz
- ◆ 输出电压: 12V&10A
- ◆ 开关频率: 100kHz

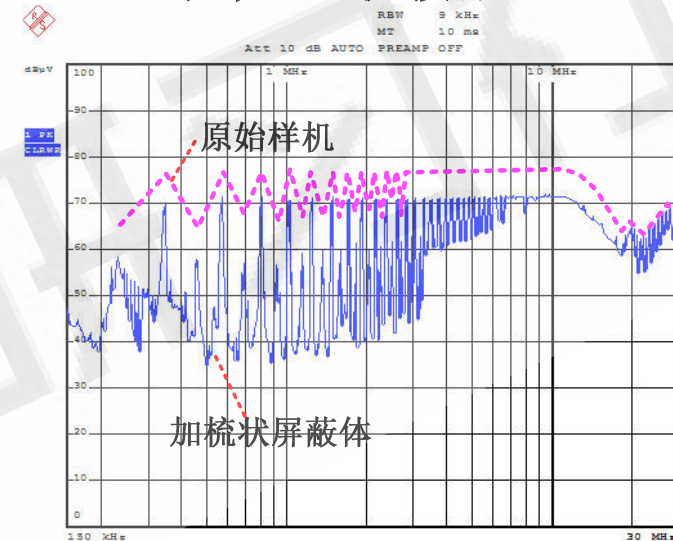


实验样机变压器结构:

磁芯: PQ35/35; 原边: 35匝; 副边: 2匝



传导共模噪声测试实验结果: (不带EMI滤波器)



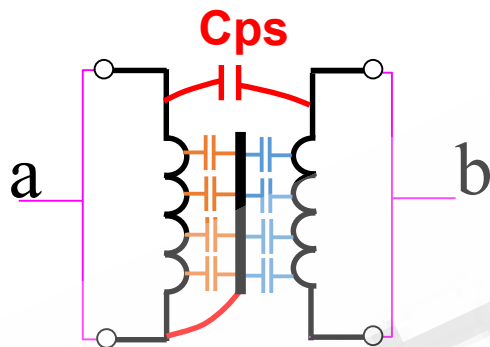
加梳状屏蔽体后在**150kHz~20MHz**范围内改善了约**4~10dB**。

应用实验结果表明:

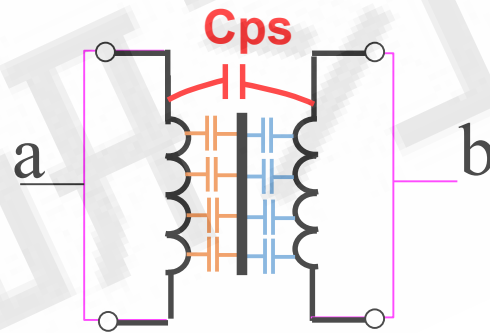
- 梳状屏蔽体具有良好的电场屏蔽效果;
- 不影响变压器的电磁参数。

□ 实验结果验证了梳状电场屏蔽体的实际有效性和可行性

LCR表/阻抗分析仪等（二端/单端口）



☹ $C_{ab} = C_{ps} + C_{shs}$

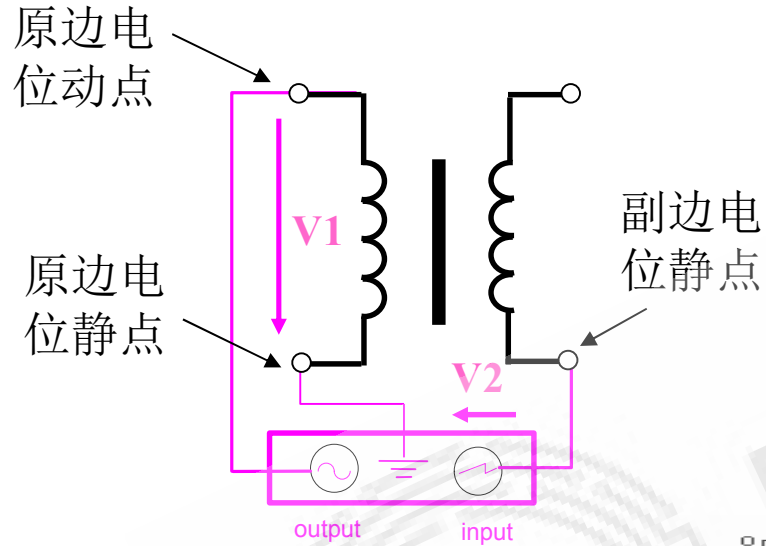


☹ $C_{ab} = C_{ps} + C_{shp} // C_{shs}$

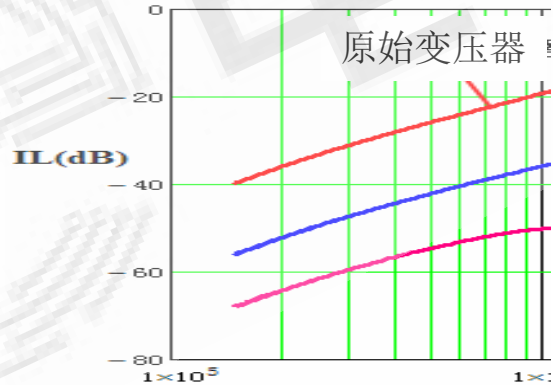
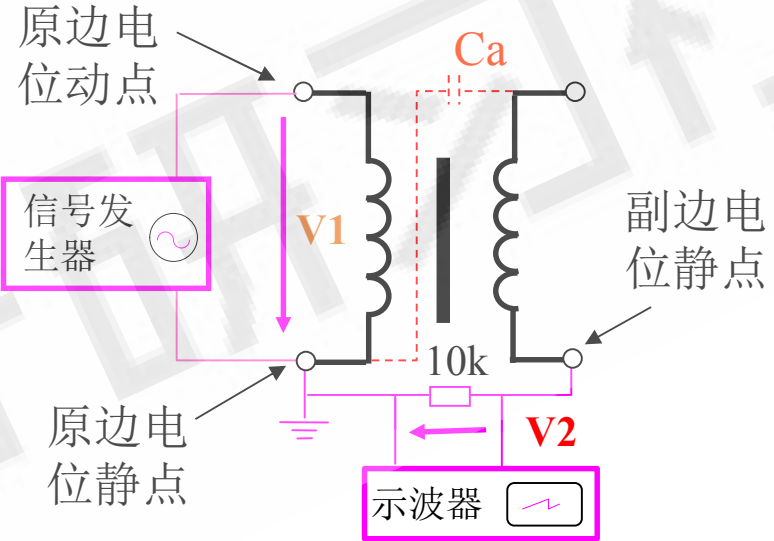
- 沿着绕组导体上的电压分布不均匀
- 原副边绕组之间有屏蔽

➔ 用LCR表无法表达

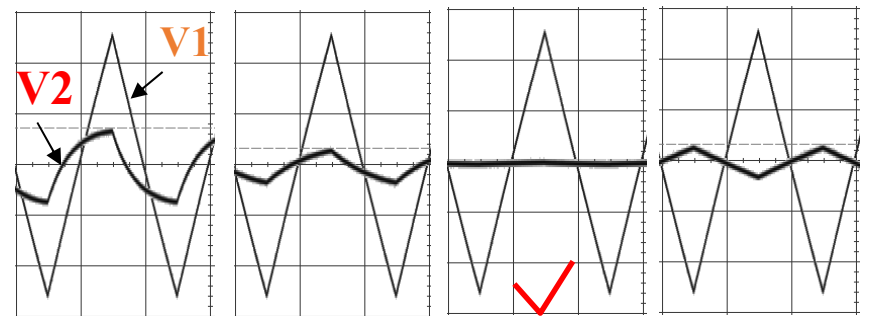
网络分析仪



信号发生器+示波器



不同屏蔽结构设计



Ca=0 → Ca增大 →



谢谢!
Q & A