西安交通大學

XI'AN JIAOTONG UNIVERSITY

氮化镓器件的应用与集成化

裴云庆
西安交通大学

电子研习社

提纲

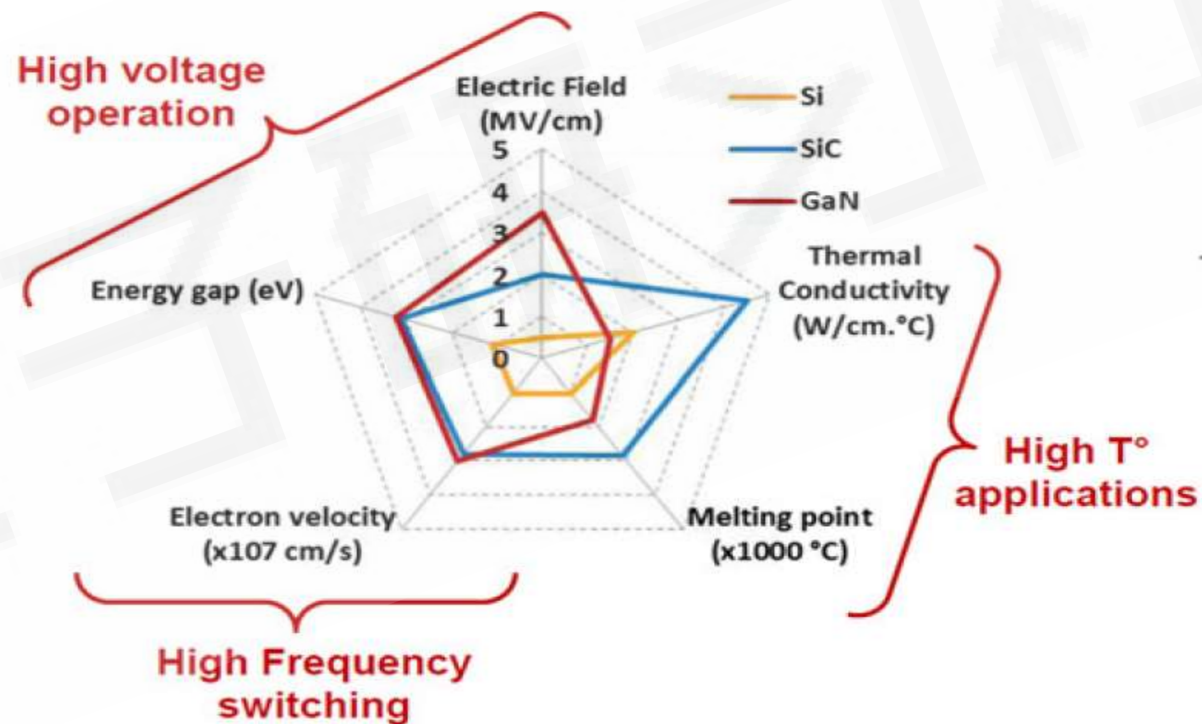
- 氮化镓器件的特性
- 氮化镓器件的驱动
- 功率回路的优化
- 基于氮化镓器件的集成化

电子研习社

GaN 和SiC材料性能的优势

- 宽禁带半导体材料
  - GaN, SiC ...

- GaN vs. Si材料性能优势
  - 禁带宽
  - 击穿场强高
  - 电子迁移速度快

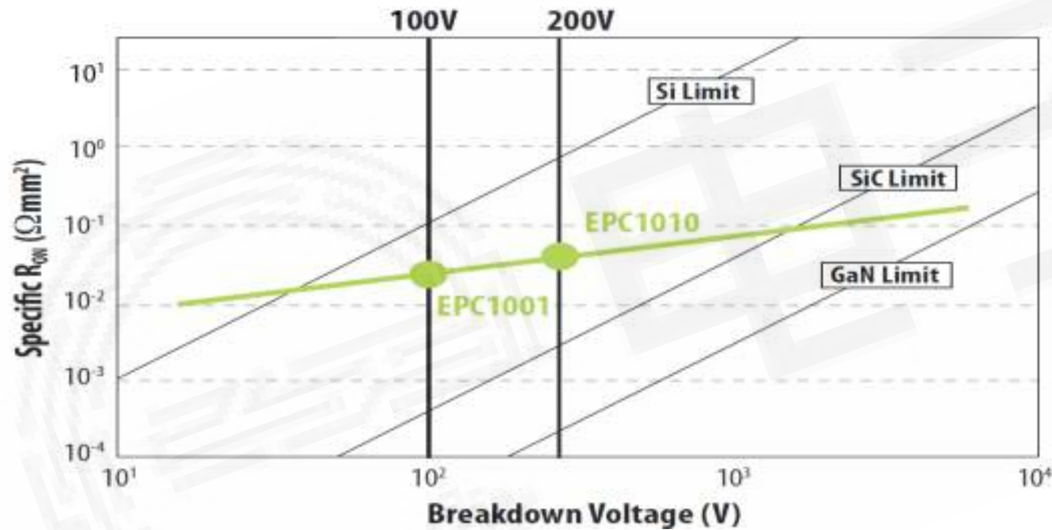


Jose Millan, Philippe Godignon, Xavier Perpin`a, Amador Perez-Tomas, and Jose Rebollo. A Survey of Wide Bandgap Power Semiconductor Devices. IEEE TRANSACTIONS ON POWER ELECTRONICS, VOL. 29, NO. 5, MAY 2014

宽禁带材料器件的性能预期

- 通态电阻更低
- 开关速度更快

导通电阻



击穿电压

高电压GaN vs. Si MOSFET

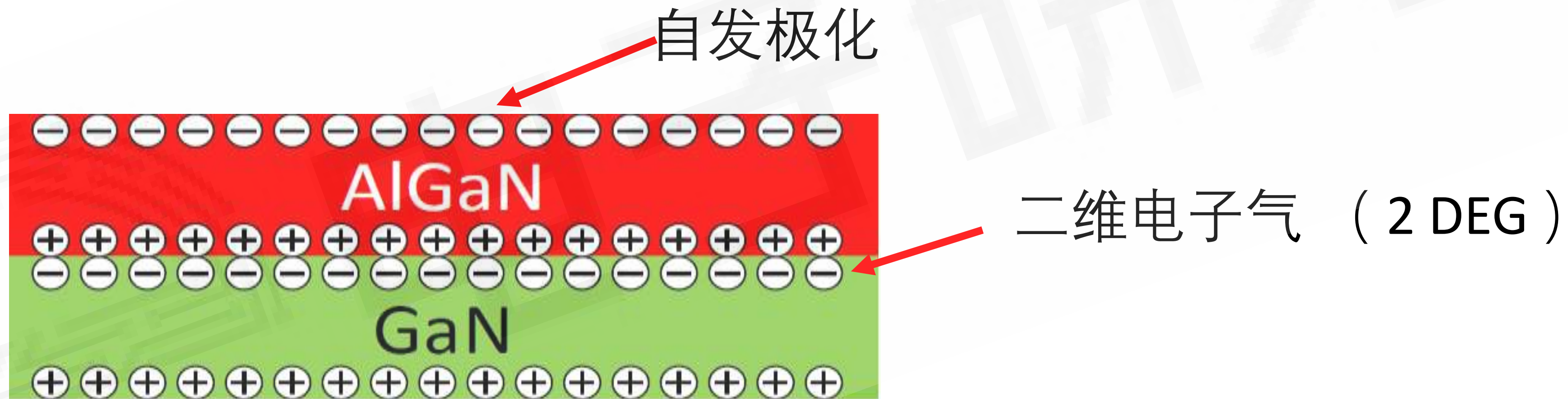
GaNSystems

Device	Vds	Rds(on)	Qg	FOM
GaNSystems GS66516T	650V	32mΩ	12nC	384
GaNSystems GS66508P	650V	63mΩ	5.8nC	365
Si CoolMos IPB65R045C7	650V	45mΩ	93nC	4185
Si CoolMos IPW65R019C7	650V	19mΩ	215nC	4085

*GaN Transistors for Efficient Power Conversion, April 22,2013, Design west, EPC Co.

GaN器件的基本结构

- GaN器件导电的基本原理—二维电子气

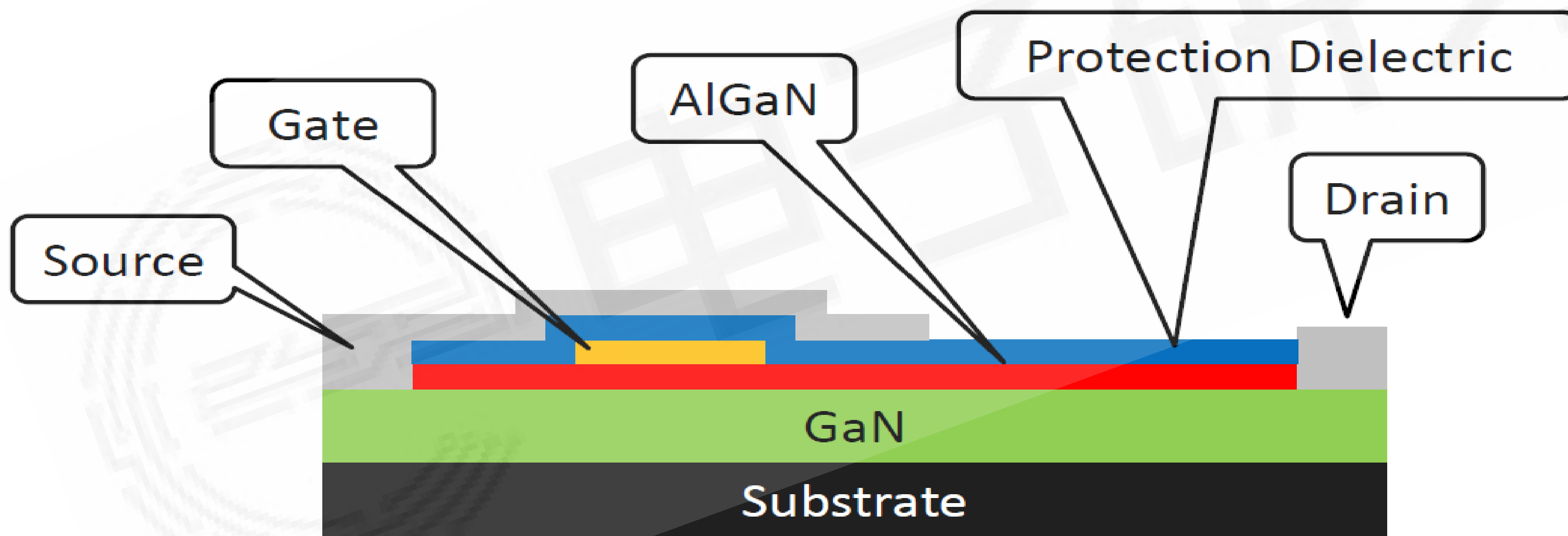


GaN 导电的基本原理

*Documents from EPC, GaN Transistors for Efficient Power Conversion,2013, Design west, EPC Co.

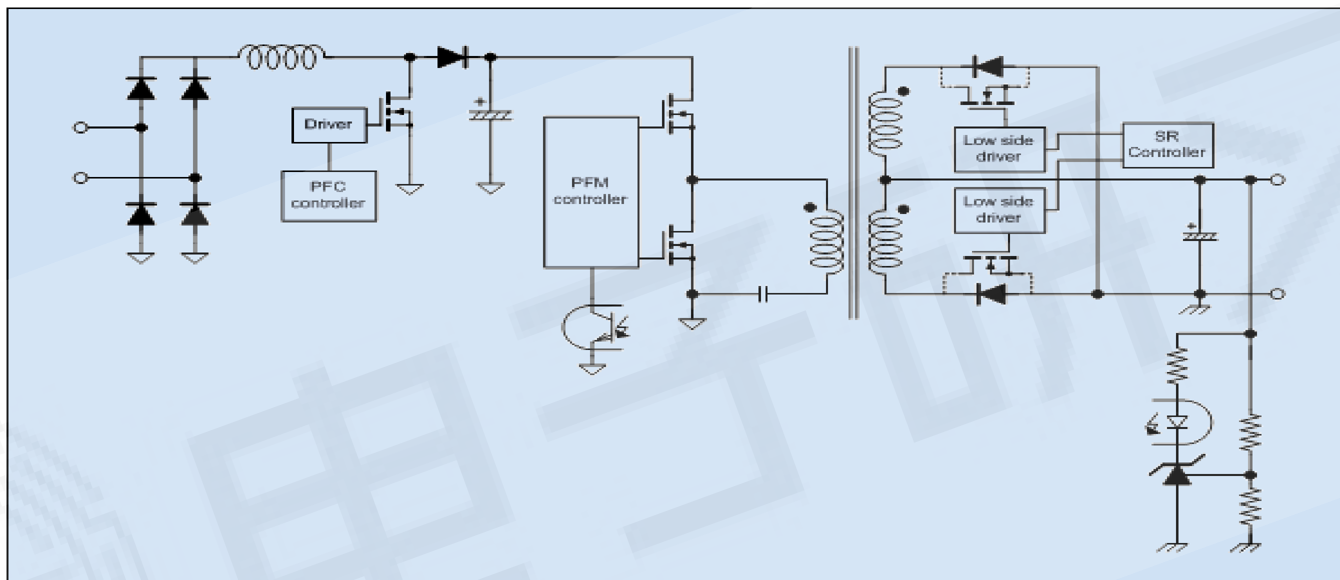
GaN器件的基本结构

- 耗尽型GaN器件（常通型）



GaN器件的基本结构

- 常通型器件的问题



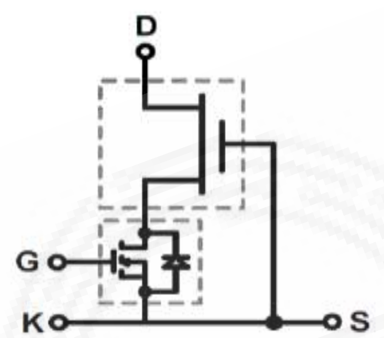
- 死循环
  - 上电前控制电路需要先行通电，使GaN器件关断，否则就会造成短路；
  - 存在短路的情况下，控制电路的供电电路无法启动。

问题：常通型器件难以直接应用

常断型的GaN器件/Cascode（共栅）器件

transphorm
TPH3006LD

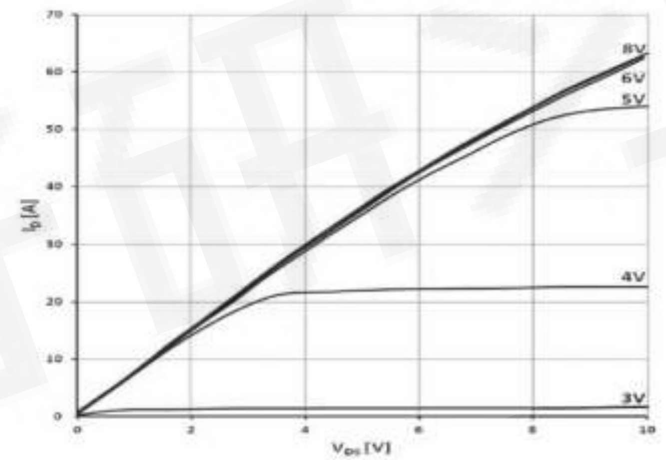
GaN Power
Low-loss Switch

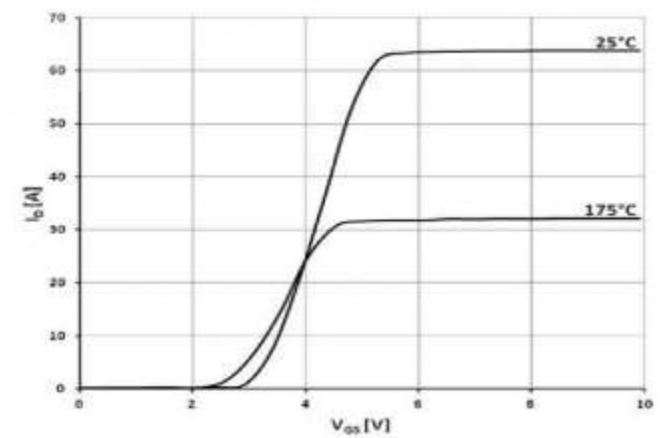


8x8 PQFN Package

PRODUCT SUMMARY (TYPICAL)	
V_{DS} (V)	600
$R_{DS(on)}$ (Ω)	0.15
Q_{rr} (nC)	54

Gate curves

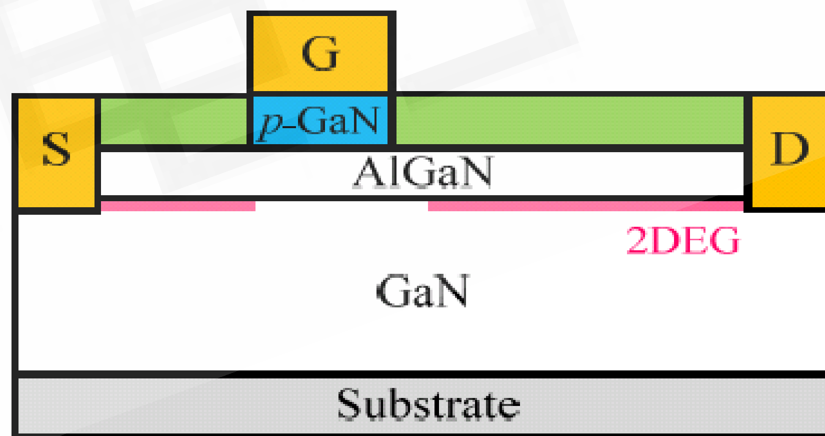




- From manufactures' webpage and based on opened materials

常断型GaN器件——eGaN

- p 型栅结构方案是利用栅极下方的p 型（Al）GaN 层抬高沟道处的势垒，从而耗尽沟道中的2DEG 来实现常断状态。



p 型栅结构

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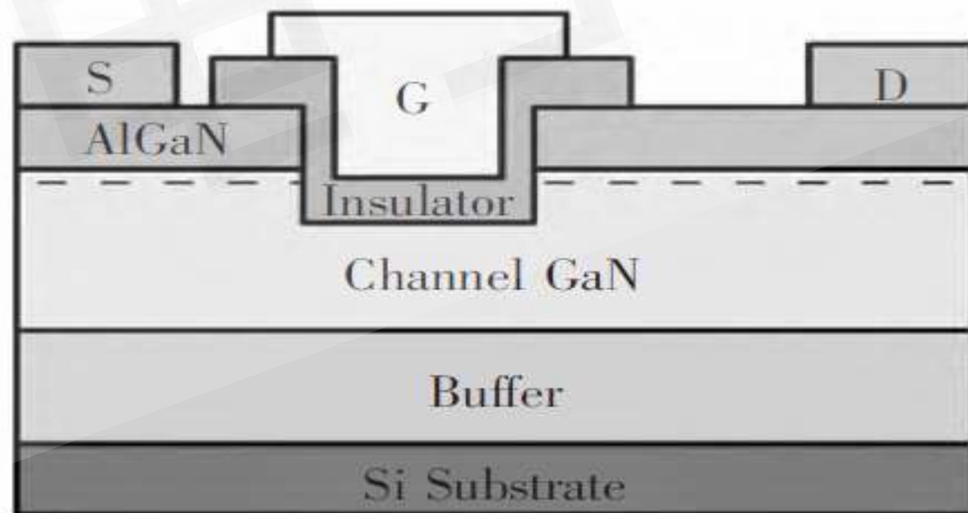
常断型GaN器件——eGaN

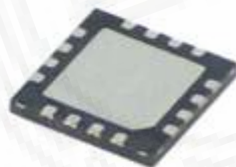
- 通过凹槽切断栅极下方的2DEG，使得器件在零栅压下为关断状态。当正栅压增至大于阈值电压时，将在栅界面处形成电子积累层以作为器件的导电沟道，器件呈导通状态。



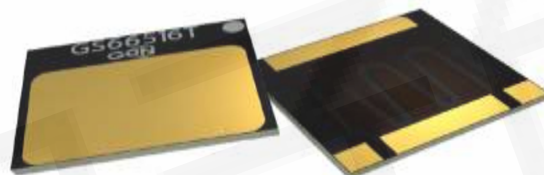
常断型GaN器件——eGaN

15-200V

Panasonic

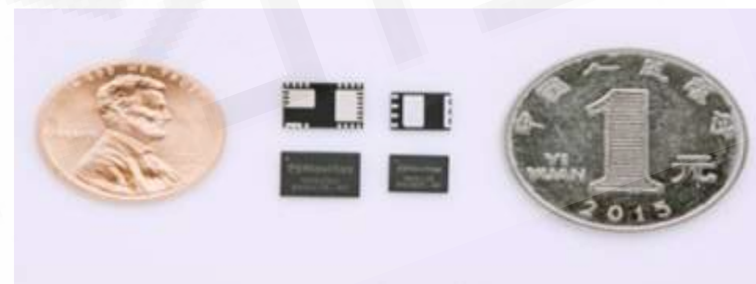


600V



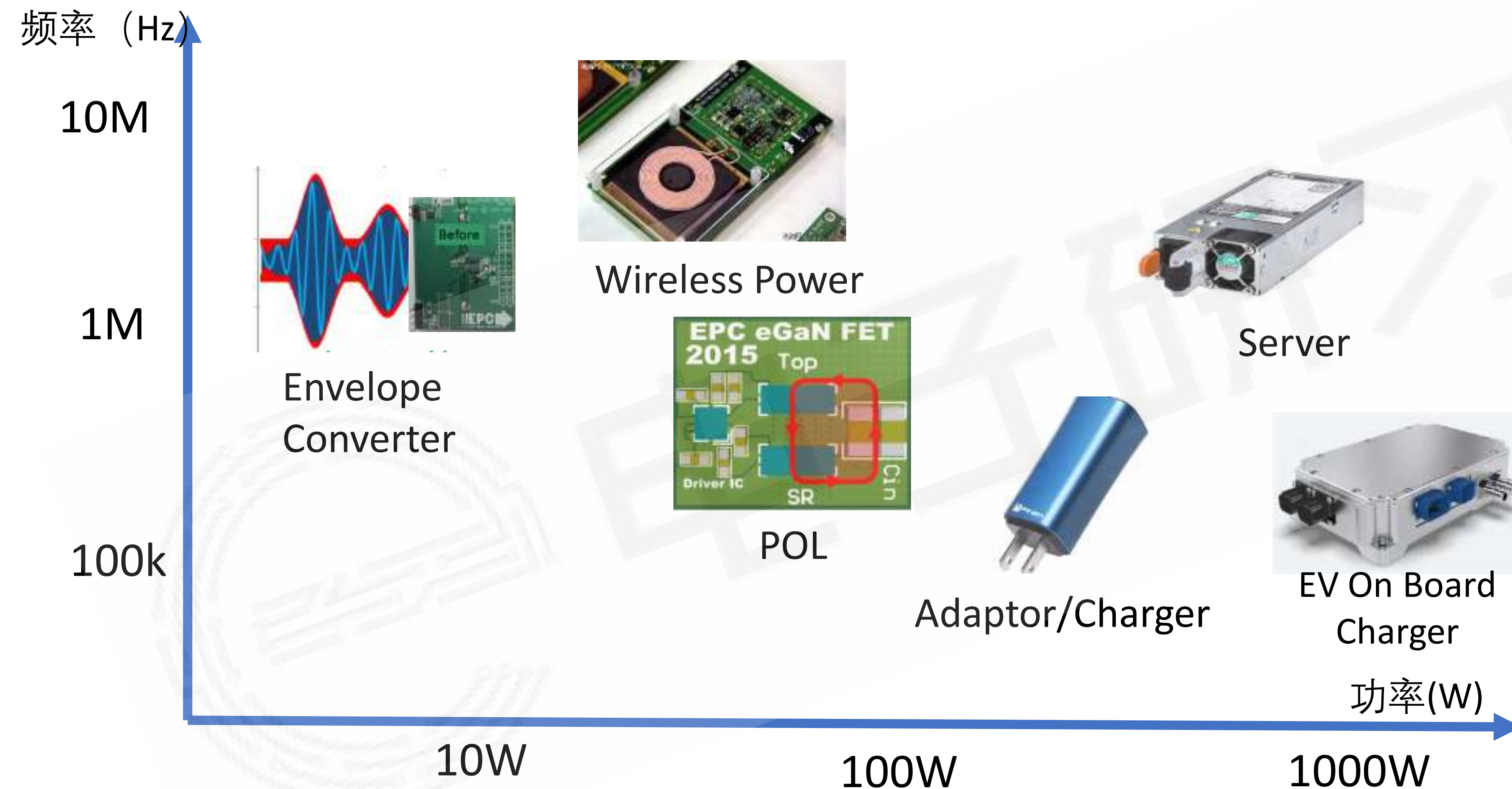
100 / 650V

CoolGaN
600V



GaN Power IC

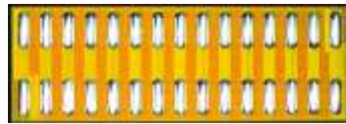
GaN器件的适用范围



GaN器件适用于中小功率、高开关频率的场合。

GaN器件的特性——低通态电阻

低电压GaN vs. Si MOSFET



EPC

Device	Vds	Rds(on)	Package
EPC EPC2023	30V	1.45mΩ	LGA 6.05 x 2.3
Si Mos BSC0500NSI	30V	1.3mΩ	SuperSO8 5.15 x 5.95
EPC EPC2047	200V	10mΩ	BGA 4.6 x 1.6
Si Mos IPB107N20N3G	200V	10.7mΩ	TO-263 8.5x9.8 DieSize：5x6

高电压GaN vs. Si MOSFET

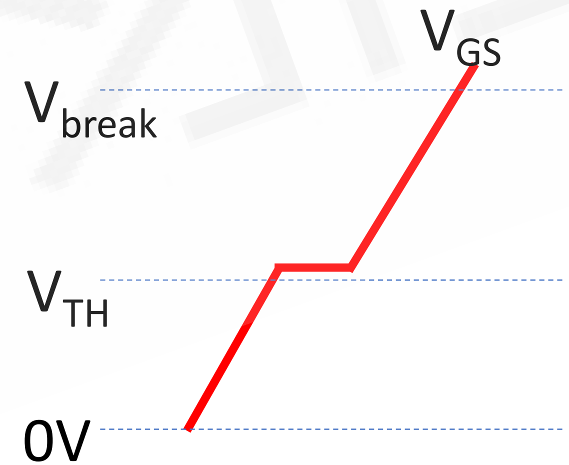
GaNSystems

Device	Vds	Rds(on)	Dimensions
GaNSystems GS66516T	650V	32mΩ	9.0x7.6x0.54 mm
GaNSystems GS66508T	650V	63mΩ	6.9x4.5x0.54 mm
Si CoolMos IPB65R045C7	650V	45mΩ	TO-247
Si CoolMos IPW65R019C7	650V	19mΩ	TO-247

eGaN器件特性——栅极电压V_{GS}特性

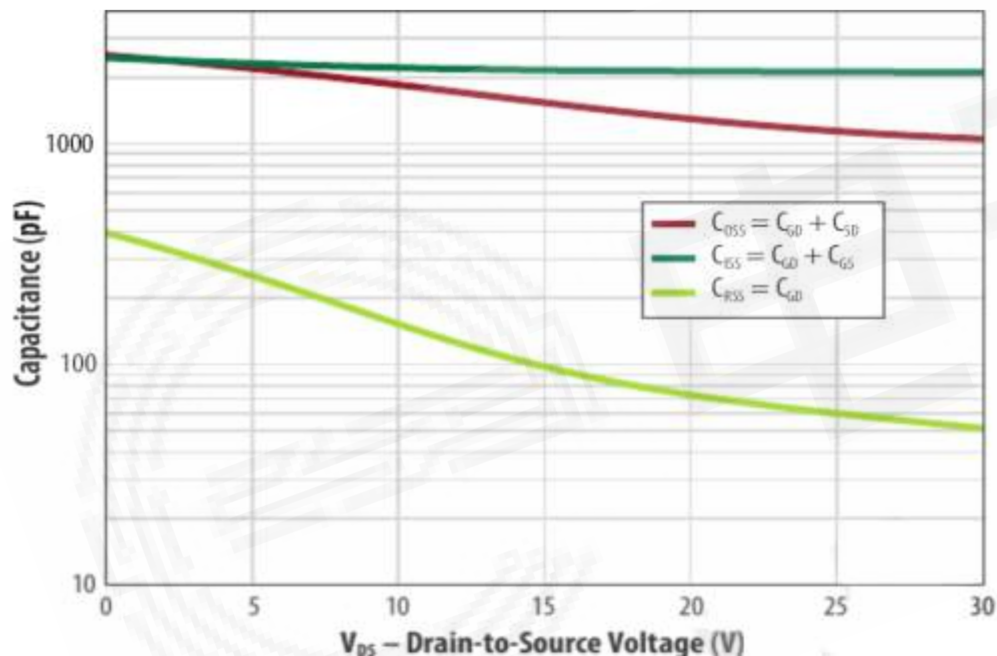
- Vgs 击穿电压低于 Si MOSFET，电压容限小.
- 阈值电压低，对噪声敏感.

	Si MOSFET	eGaN		
型号	BSC0500NSI	EPC2023	EPC2047	GS66508T
电压	30	30	200	650
栅极电压	-20 ~ +20	-4 ~ +6	-4 ~ +6	-10 ~ +7
阈值电压	1.2~2	0.7 ~ 2.5	0.8~2.5	1.1 ~ 2.6
全导通电压	4~5	4.5~5.5	4.5~5.5	6
电压裕量	15	0.5	0.5	1

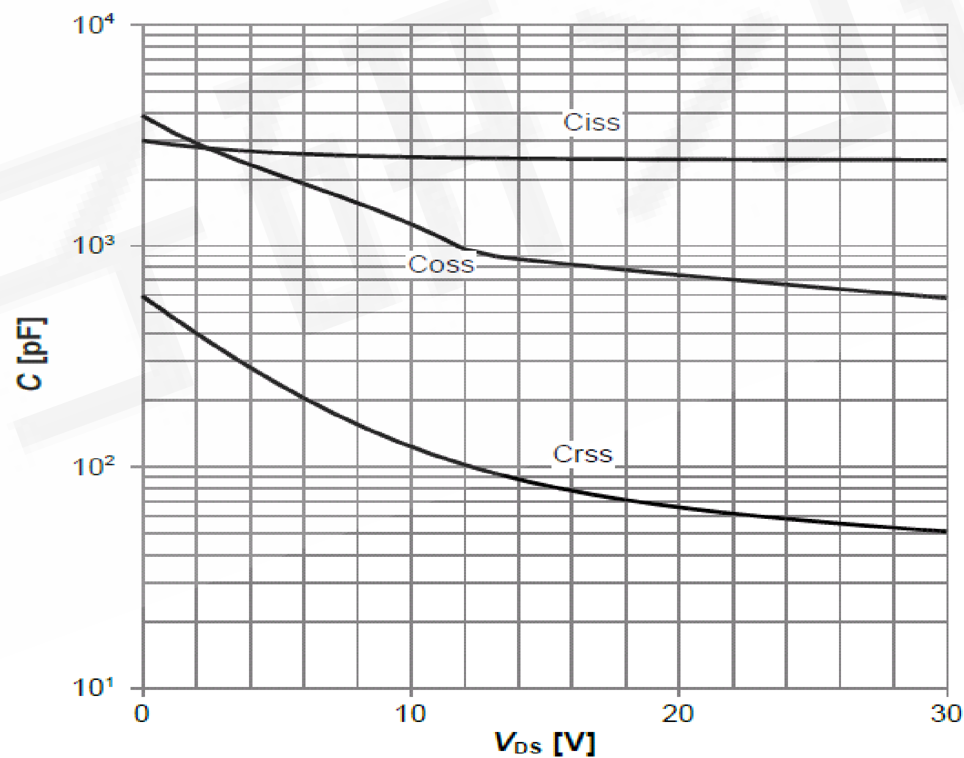


eGaN的特性-结电容 (30V)

- 结电容远小于硅器件



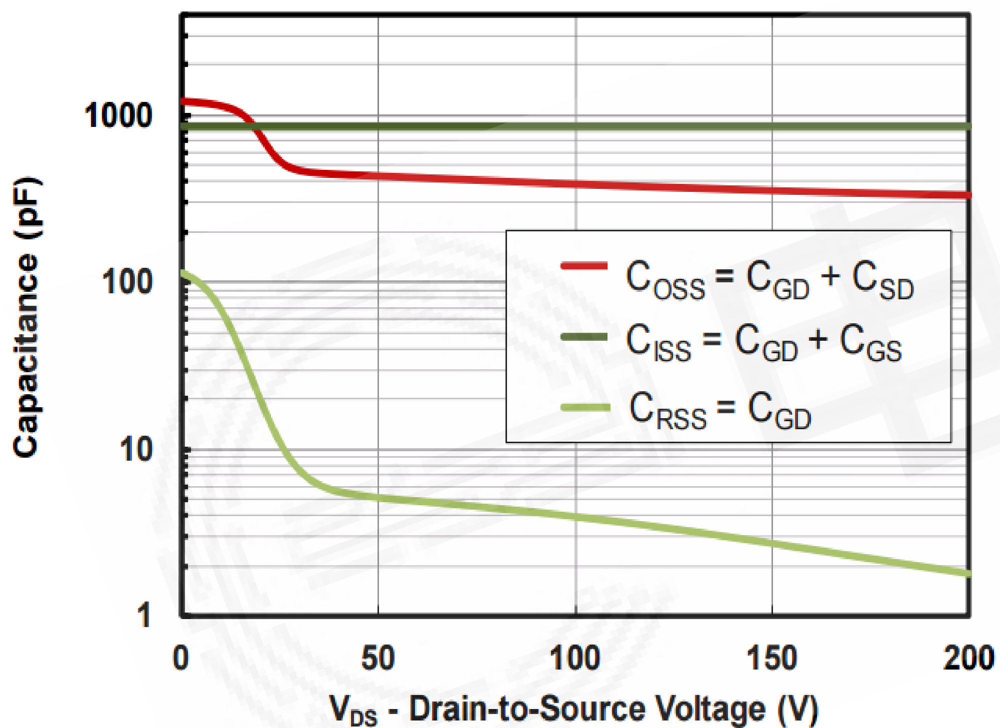
eGaN EPC2023 30V 1.45mΩ



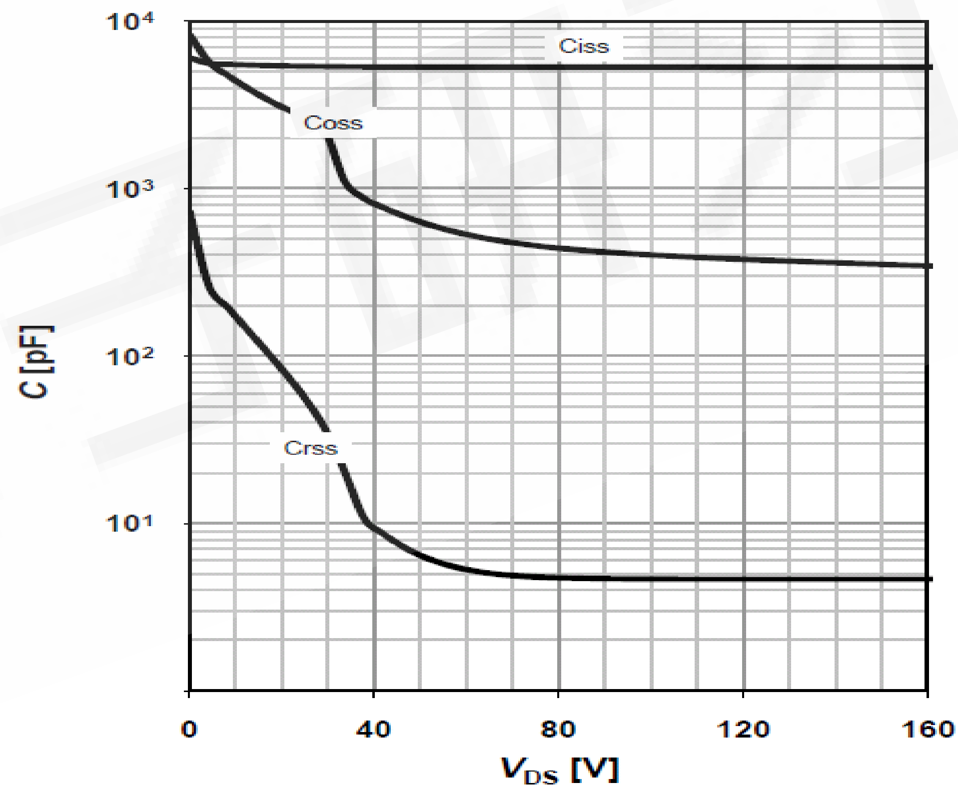
Si BSC0500NSI 30V 1.3mΩ

eGaN的特性-结电容(200V)

- 结电容远小于硅器件



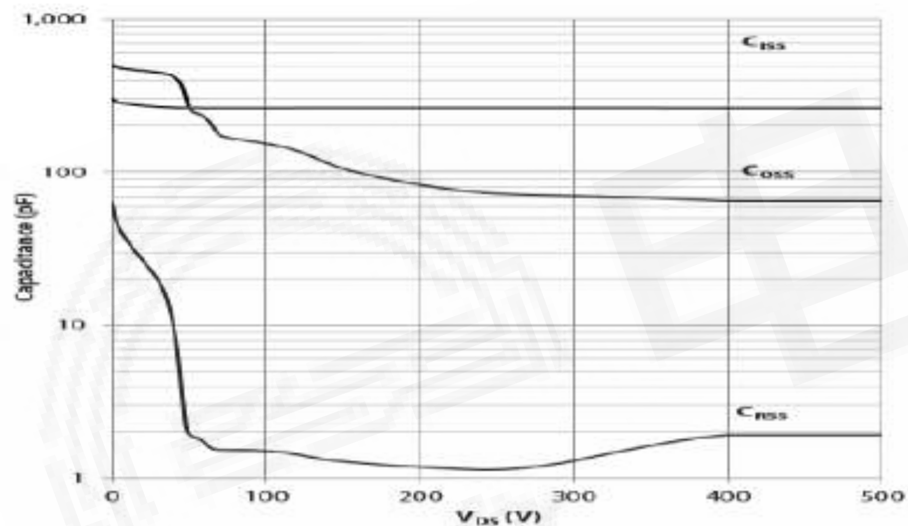
eGaN EPC2047 200V 10mΩ



Si IPB107N20N3 G 200V 10.7mΩ

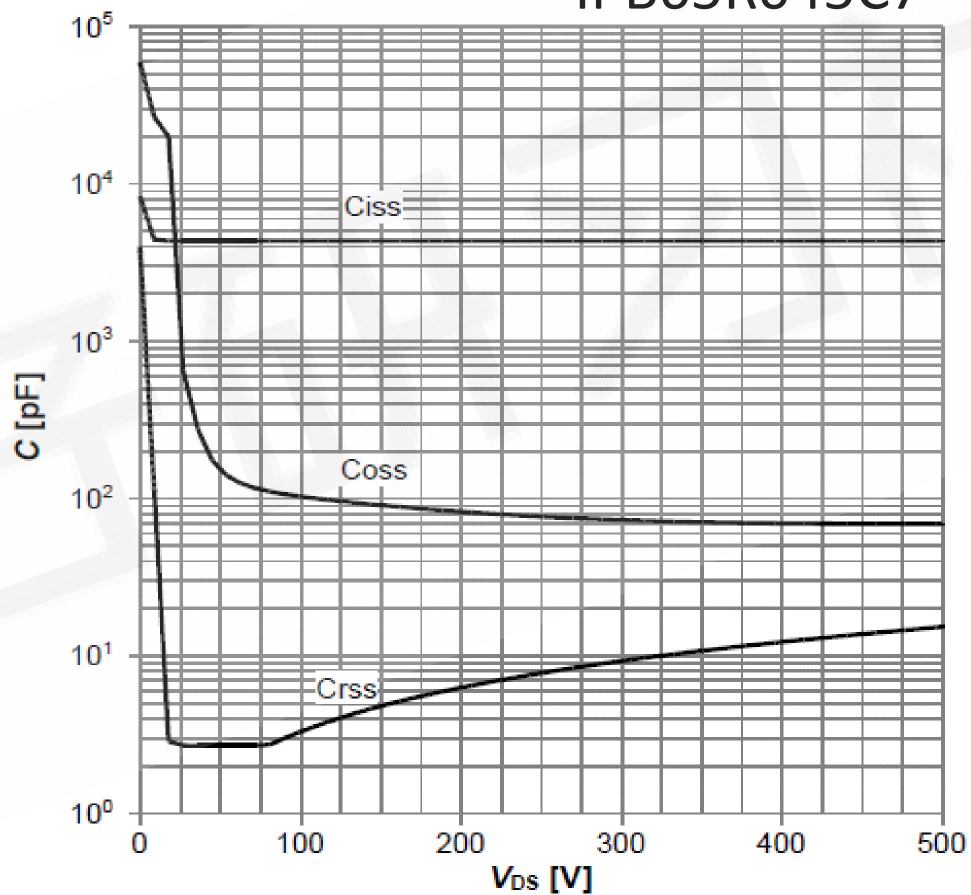
eGaN的特性-结电容(650V)

GS66508T



eGaN GS66508T 650V 63mΩ

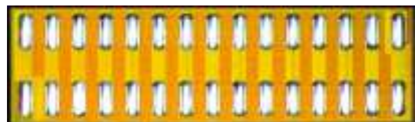
IPB65R045C7



Si IPB65R045C7 650V 45mΩ

GaN与Si器件性能比较

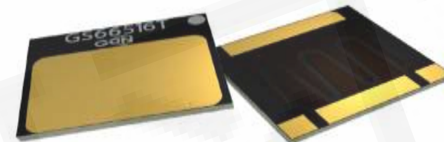
低电压GaN vs. Si MOSFET



EPC

Device	Vds	Rds(on)	Qg	FOM	Package
EPC EPC2023	30V	1.45mΩ	20nC	29	LGA 6.05x2.3
Si Mos BSC0500NSI	30V	1.3mΩ	39nC	50.7	SuperSO8 5.15 x 5.95
EPC EPC2047	200	10mΩ	8.2nC	82	BGA 4.6 x 1.6
Si Mos IPB107N20N3G	200	10.7mΩ	65nC	696	TO-263 8.5x9.8 DieSize：5x6

高电压GaN vs. Si MOSFET



GaNSystems

Device	Vds	Rds(on)	Qg	FOM
GaNSystems GS66516T	650V	32mΩ	12nC	384
GaNSystems GS66508T	650V	63mΩ	5.8nC	365
Si CoolMos IPB65R045C7	650V	45mΩ	93nC	4185

低压GaN器件的通态电阻有明显优势

高压GaN器件的开关速度有明显优势

衡量功率器件的参考值：FOM=$R_{ds(on)}*Q_g$

- Qg大幅度减小的原因：
  - 结电容（Cgs，Cgd）减小5倍
  - 栅极电压减小2倍（V^2减小4倍）

eGaN器件栅极特性小结

- 栅极击穿电压更低
- 阈值电压更低
- 栅极电荷Qg更低
- 优点:
  - 需要的驱动电流小
  - 驱动损耗小 （$1/2CV^2$）
  - 高开关频率、低开关损耗
- 缺点
  - 栅极电压裕量低，对栅极过电压较为敏感
  - 产生强EMI干扰和过电压尖峰
  - 栅极信号中噪声和寄生振荡也很强（高压eGaN器件显著）

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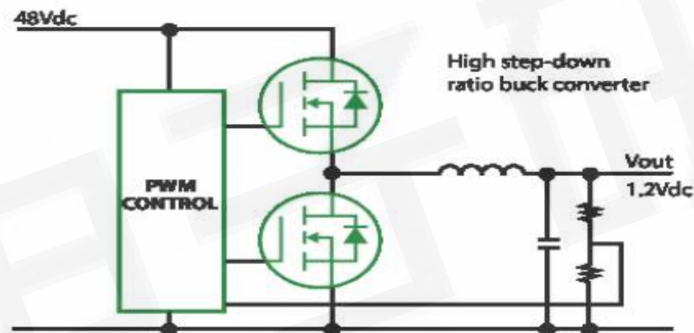
发挥GaN器件的性能优势

- 低压器件（<200V）导通电阻优势显著
  - 典型应用：
    - SYNC Buck

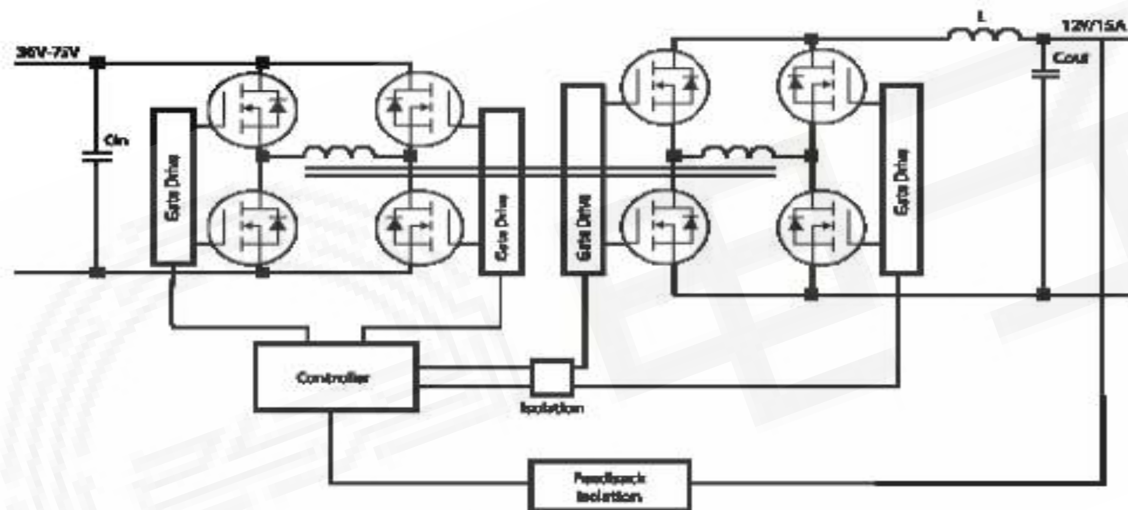


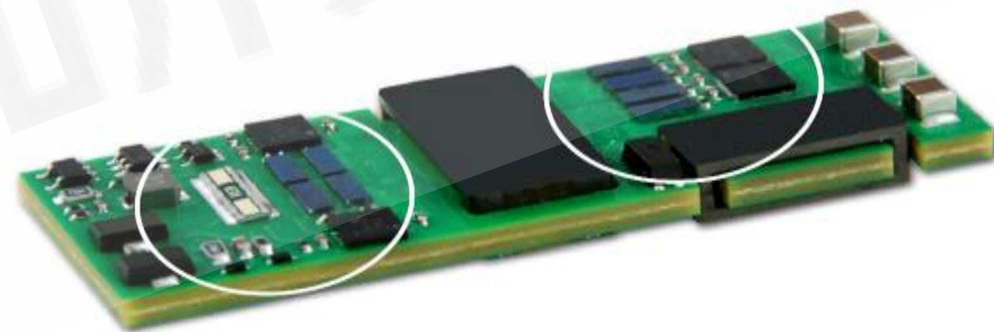
用硅器件构成的Buck

用eGaN器件构成的Buck

发挥GaN器件的性能优势

- 低压器件（<200V）典型应用
  - 隔离DC/DC变换器



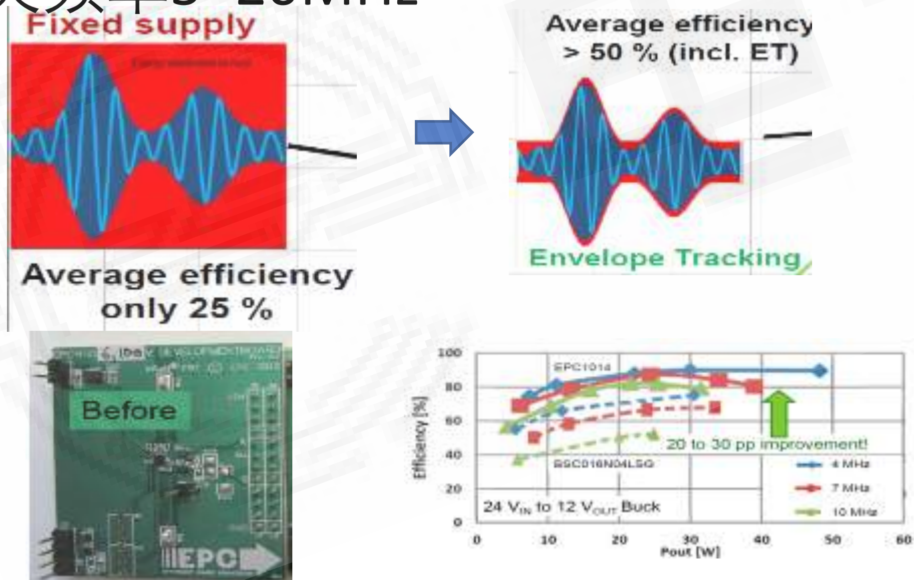


如何发挥GaN器件的性能优势

- 低Qg、低开关损耗的优势
  - 提高开关频率5-10倍
  - 带来的好处：
    - 电路中磁性元件、谐振电容的体积按照比例相应减小
    - 频率提高到一定程度，可以利用分布参数甚至全部使用分布参数构成电路了

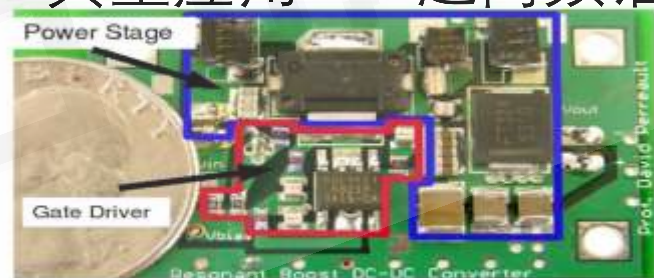
典型应用1： Envelope Converter

- 开关频率5~20MHz



*DesignWest 2013 GaN Seminar from EPC Co.

典型应用:2： 超高频谐振变换器



MIT： 110MHz VHF converter

XJTU： 30MHz Boost

GaN器件应用中的难点问题

- 驱动的问题
  - 驱动电压
  - 驱动回路设计与器件稳定性
- 回路电感的问题:
  - 提高频率的障碍，电感阻碍电流的变化
  - 驱动回路的电感
  - 功率回路的电感（漏极、源极回路）
- 散热的问题

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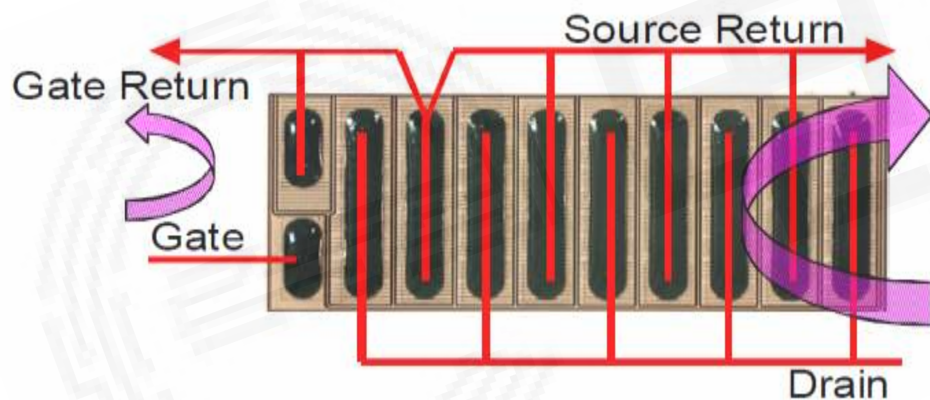
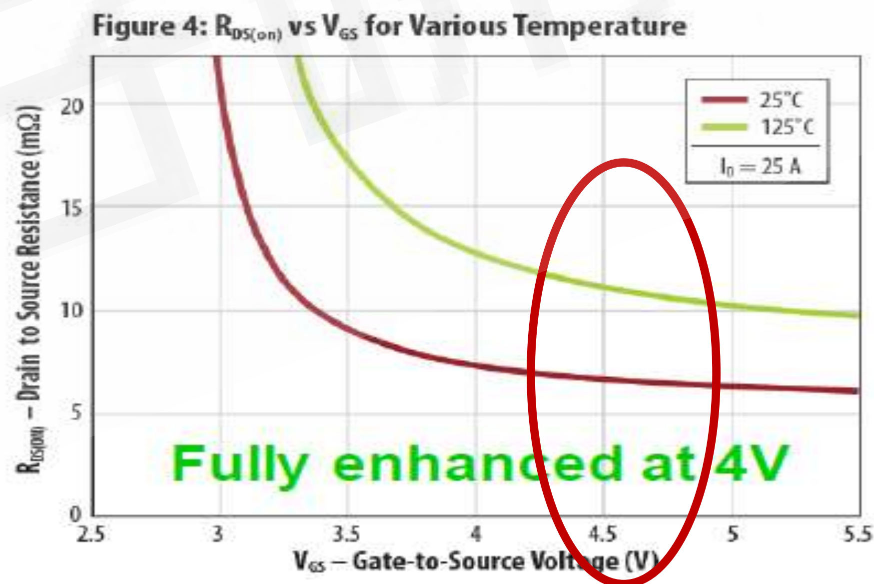
eGaN的驱动——驱动电压

- eGaN器件的栅极电压特性
  - Vgs：4~4.5V才充分导通，
  - 击穿电压：6V，栅源电压裕量较小，

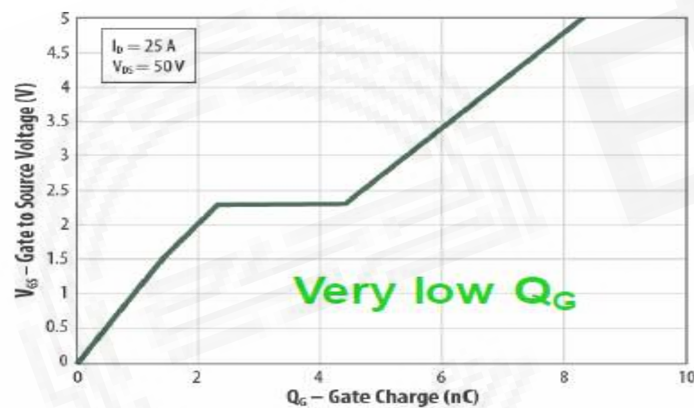




合适的驱动电压选择

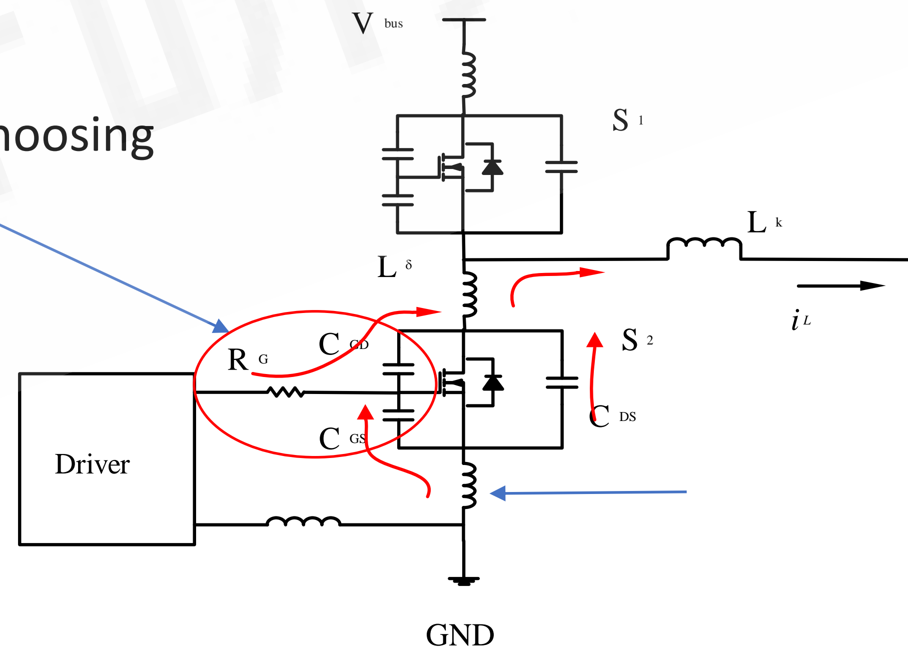
eGaN的驱动——驱动电阻

- eGaN的驱动电荷仅为Si器件的1/20，同样的驱动能力（电流），开关速度会显著提高：
  - 快速开关会因漏源回路存在寄生电感而产生过电压和寄生振荡；
  - 需要通过驱动电阻来限制驱动速度、抑制过电压、确保器件安全工作。



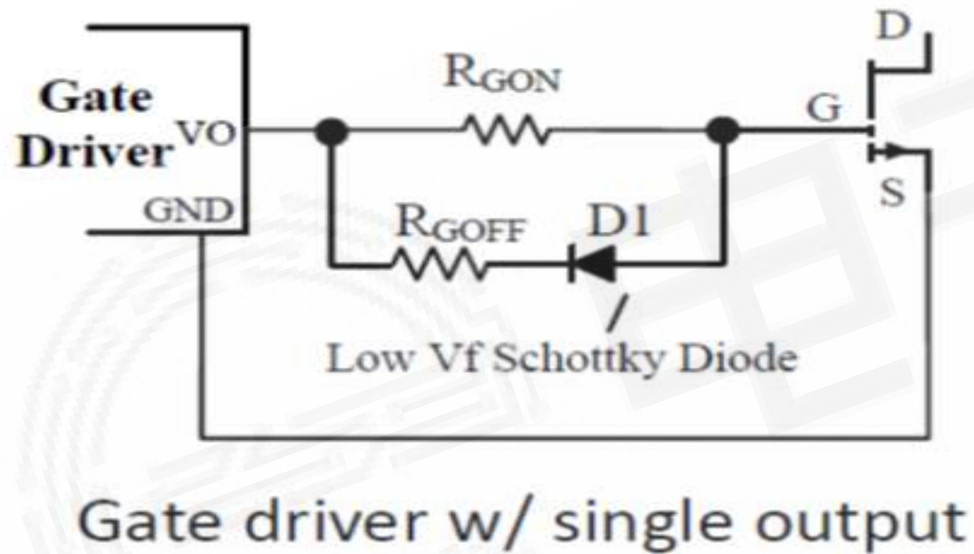
Gg：约为Si器件的1/20

Gate resistor choosing

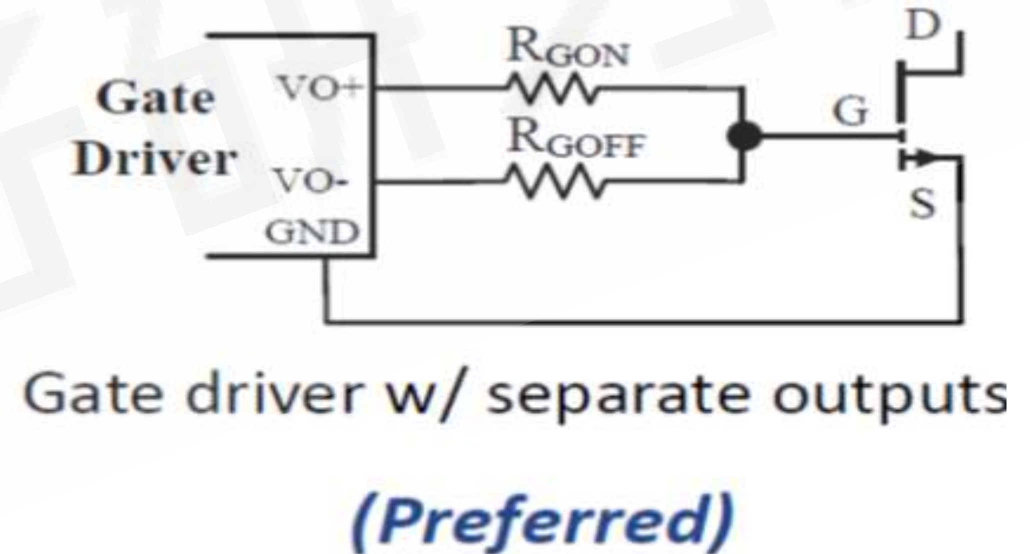


eGaN的驱动——驱动电阻

- 推荐的栅极电阻选择方案:
  - RG(ON)/RG(OFF) ≥ **5-10**



Gate driver w/ single output



Gate driver w/ separate outputs

(Preferred)

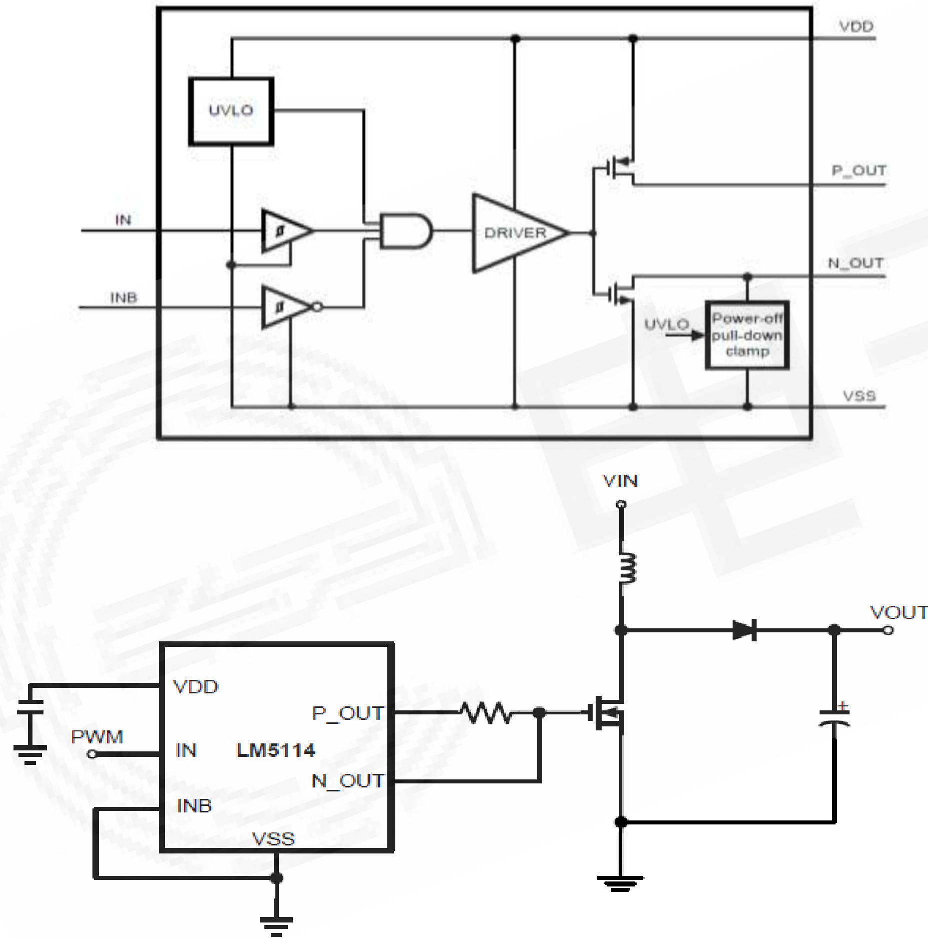
* From EPC Co.

eGaN 的驱动IC

	LM5113	LM5114	UCC27511	UCC27611
Driver Configuration	Dual Independent	Single	Inverting Non-Inverting	Inverting Non-Inverting
Peak Output Current (A)	5	7.6	8	6
Rise Time (ns)	4	12	9	9
Fall Time (ns)	4	3	7	4
Prop Delay (ns)	30	12	13	14
Input Threshold	TTL	CMOS TTL	CMOS TTL	CMOS TTL
Rating	Catalog	Catalog	Catalog	Catalog
Operating Temperature Range (C)	-40 to 125	-40 to 125	-40 to 140	-40 to 140
Package Group	DSBGA WSON	SOT-23 WSON	SOT-23	WSON
Package Size: mm2:W x L (PKG)	See datasheet (DSBGA),See datasheet (WSON)	See datasheet (WSON)	See datasheet (WSON)	See datasheet (WSON)
Approx. Price (US$)	1.49 | 1ku	0.60 | 1ku	0.49 | 1ku	0.85 | 1ku

eGaN 的驱动IC

LM5114

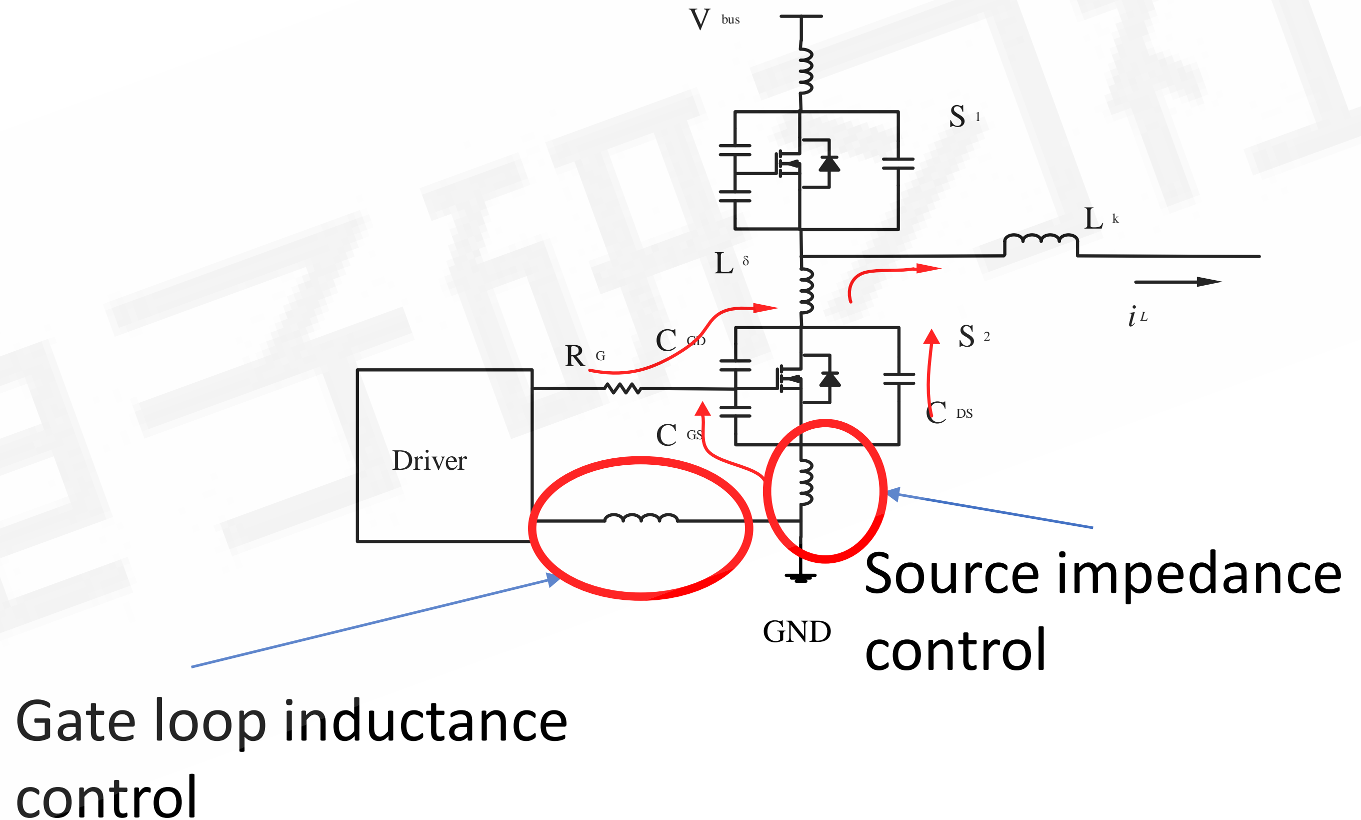


LM5114 低侧栅极驱动器的主要特性与优势:

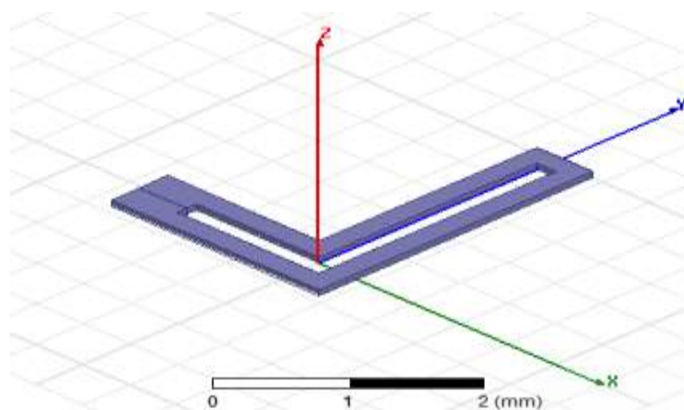
- 可优化升降时间的分离输出支持更高的效率;
- +4V 至 +12.6V 单电源支持各种应用;
- 0.23 欧姆的开漏下拉输出可避免无意接通;
- 7.6 A/1.3 A 峰值灌 / 拉电流可最大限度减少电压突变(dV/dt)的影响;
- 匹配反相及非反相输入之间的延迟时间，可降低停滞时间损耗;
- 12 ns 典型传播延迟可在提高效率的同时，支持高开关频率;
- 高达 14 V 的逻辑输入（不受 VCC 影响）；
- -40 摄氏度至 +125 摄氏度的宽泛工作温度。

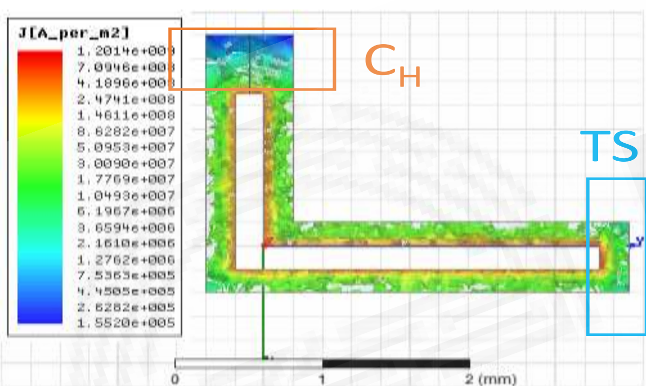
eGaN驱动回路寄生电感的抑制

- 驱动回路的电感
  - 栅极电感
  - 源极电感

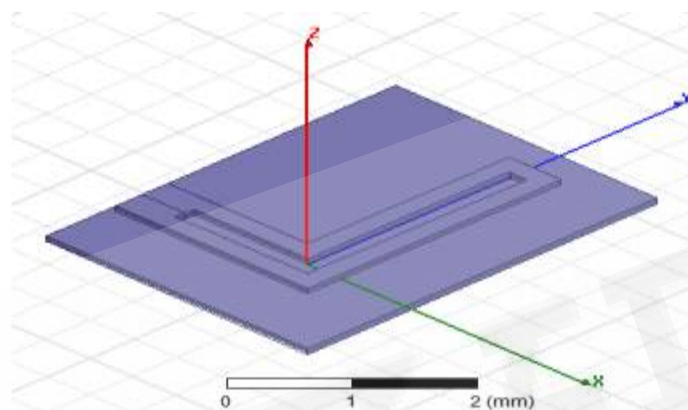


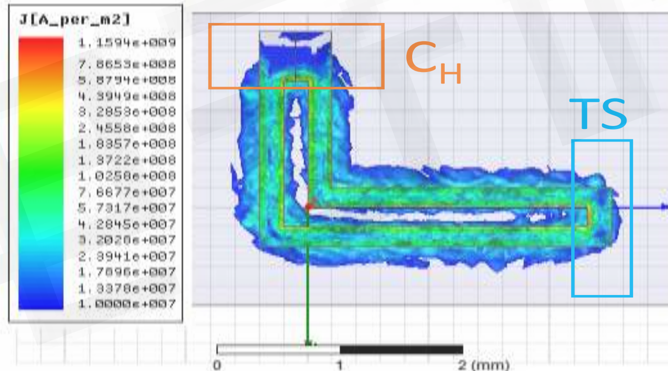
eGaN驱动回路寄生电感的抑制



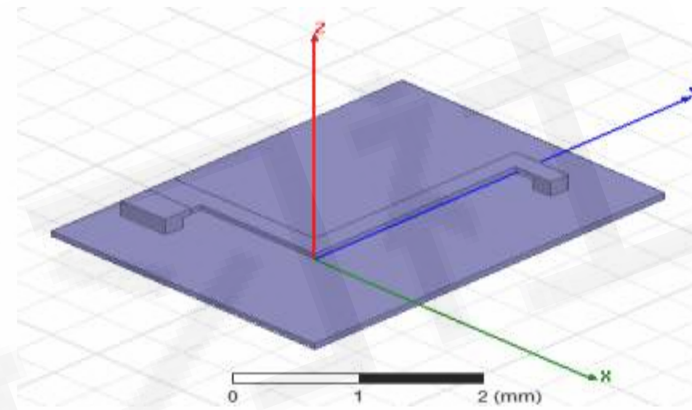


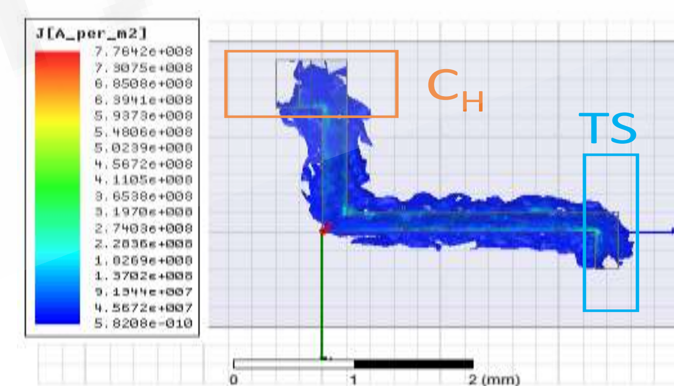
单层平行布线





单层平行布线+屏蔽层



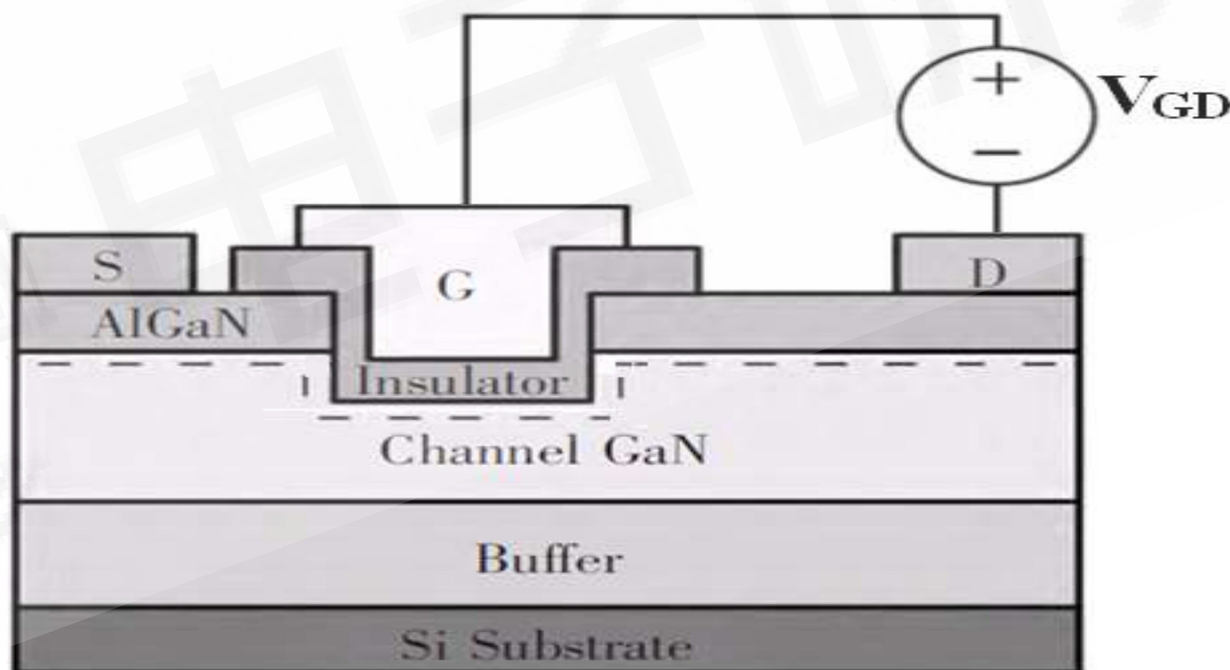


双层平行布线

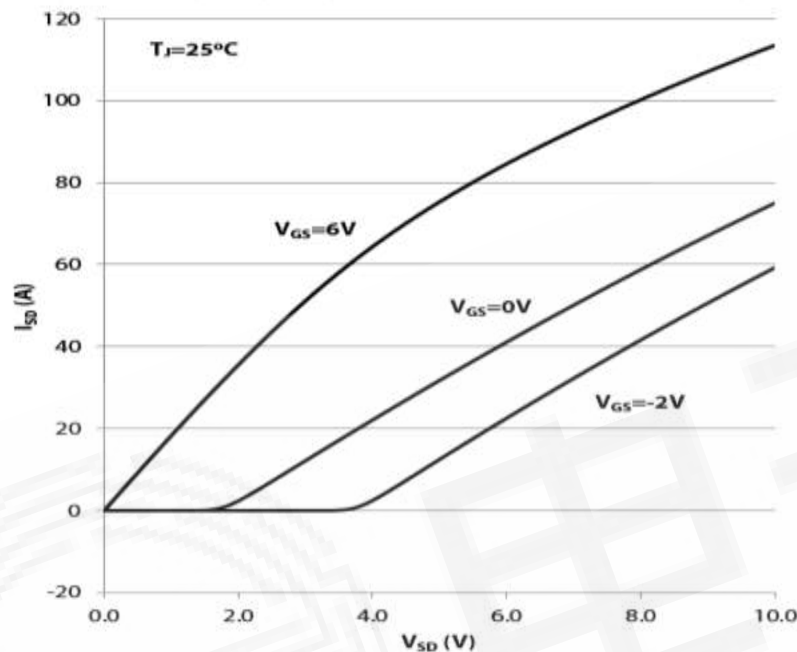
驱动回路布线方案	单层布线	带屏蔽层	双层布线
驱动回路电感	4.3nH	2.2nH	1.4nH

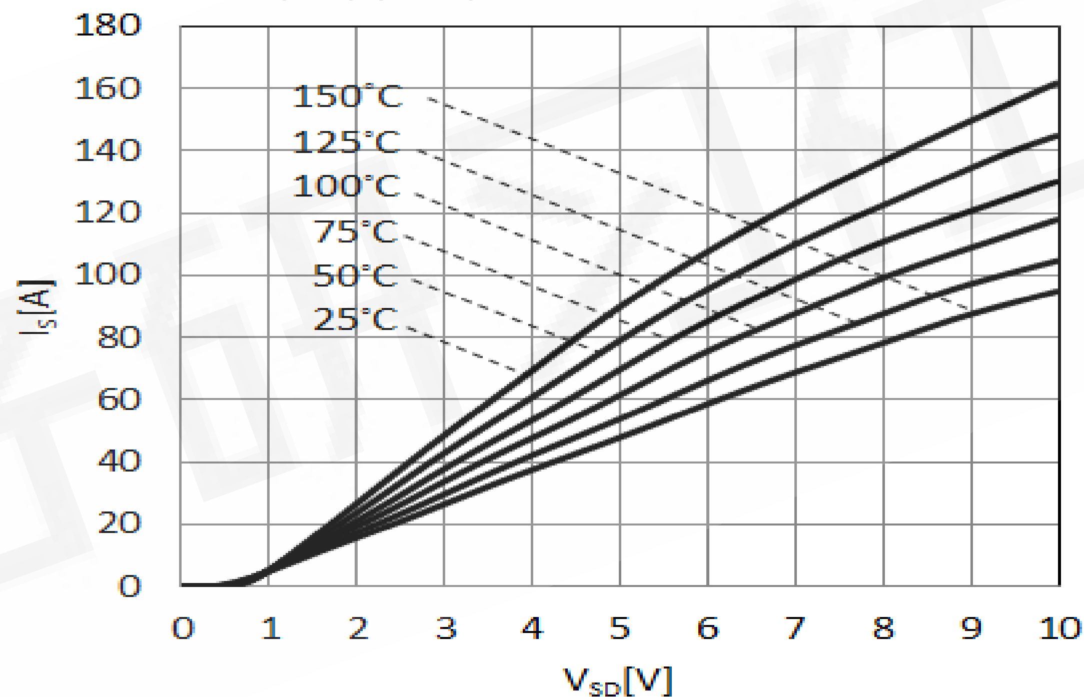
eGaN逆导通模式

- 不存在反并联的体二极管。
- 由于栅极和漏极结构的对称性，栅源电压Vgs或栅漏电压Vgd高于阈值电压Vth时，GaN晶体管均可导通。



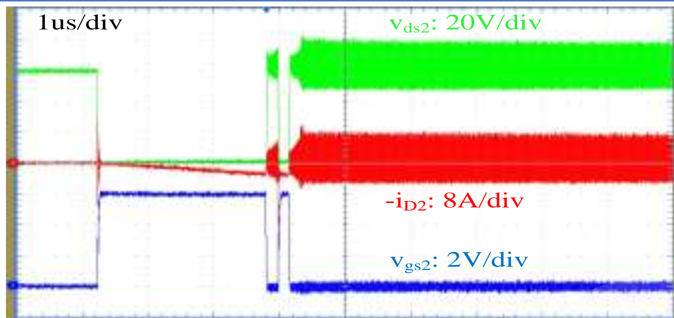
eGaN逆导通模式



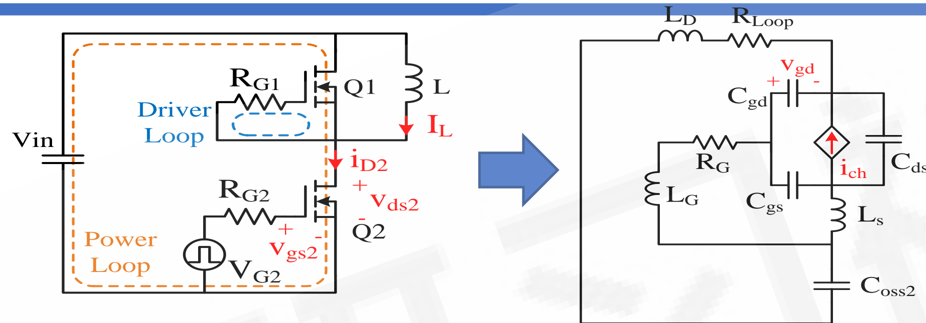


- 优点:
  - 无硅MOSFET体二极管存在的反向恢复问题
- 缺点
  - 反向导通时压降高，且与驱动电压相关，导通损耗高。
  - 容易引起自激振荡

eGaN逆导通自激振荡问题

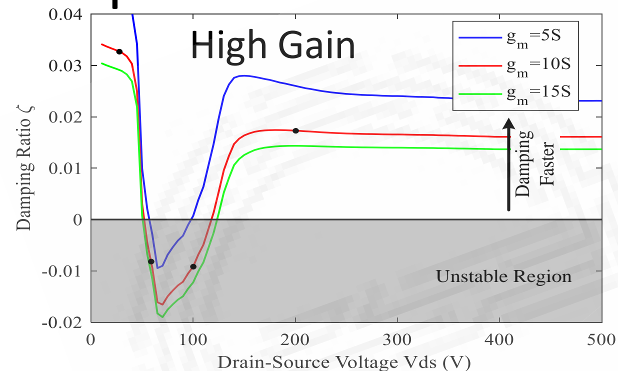


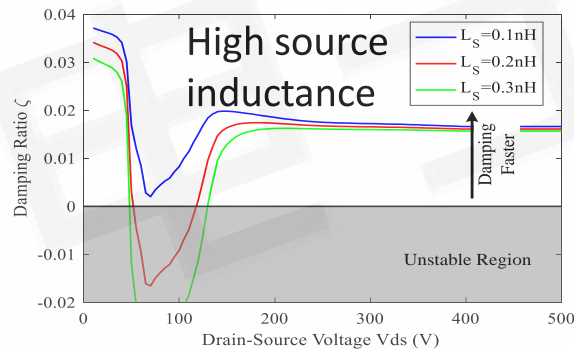
Gate voltage oscillations

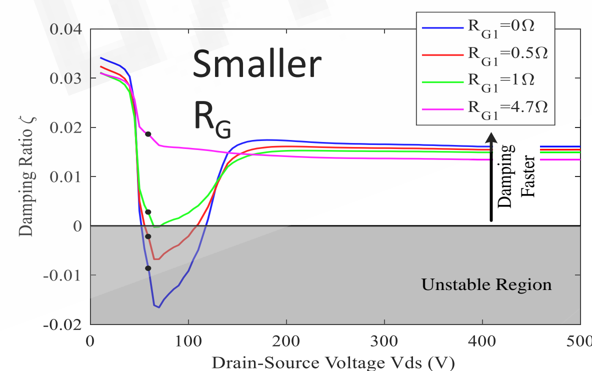


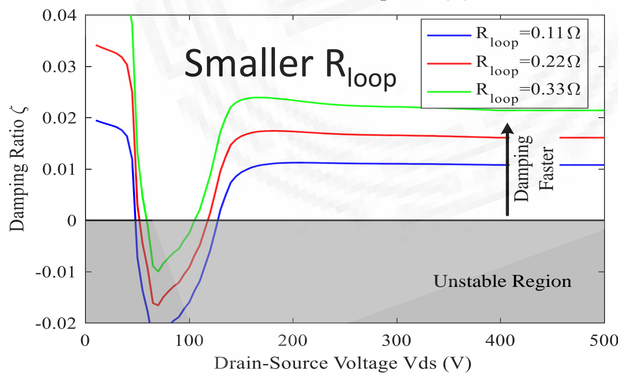
Equivalent circuit for oscillation

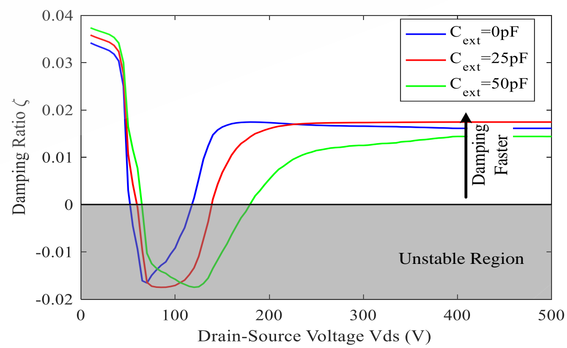
Impact factor for the oscillation:

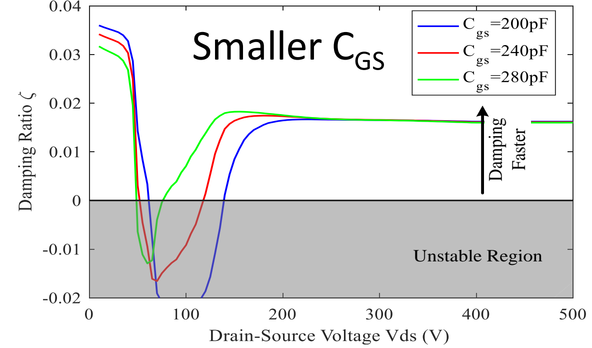






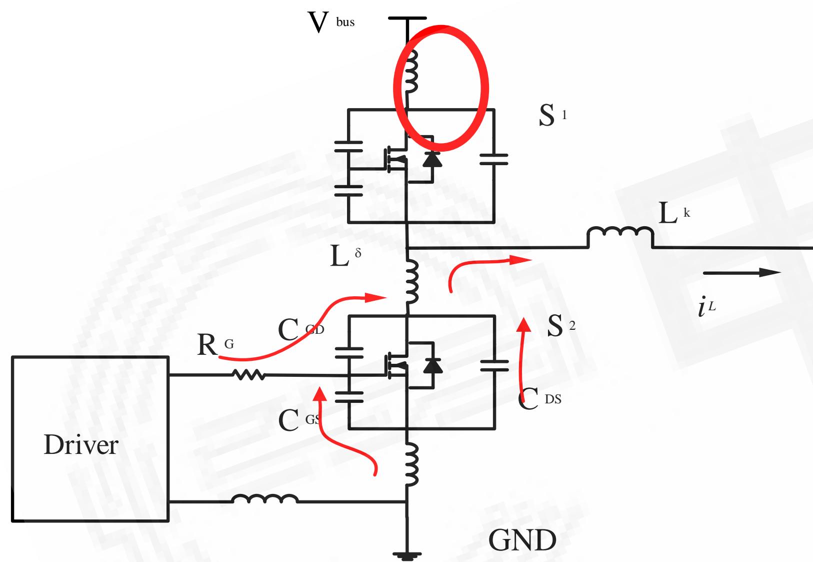






漏源回路寄生电感问题

- 漏源回路寄生电感导致的问题
  - 关断过程过电压和寄生振荡



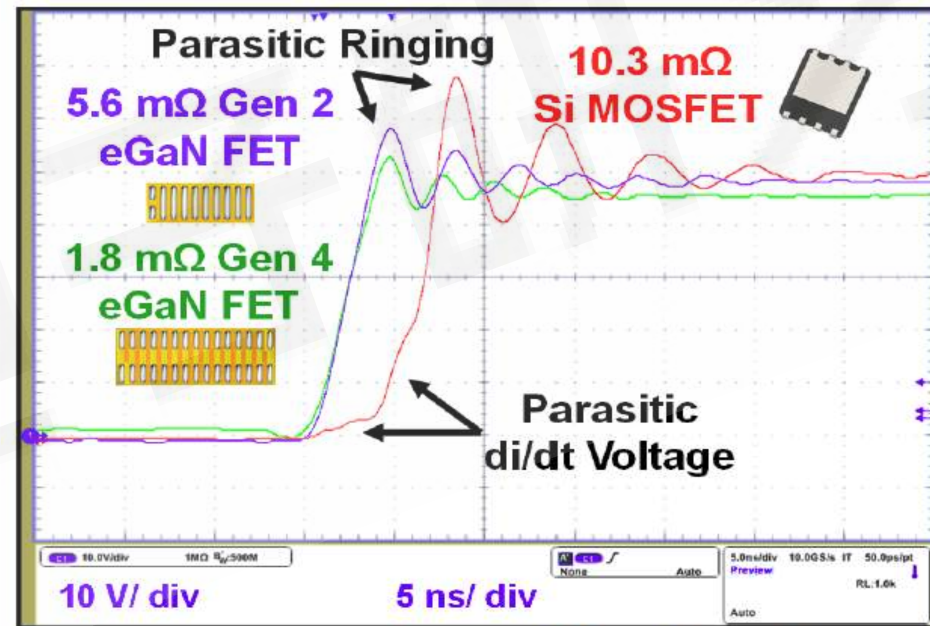


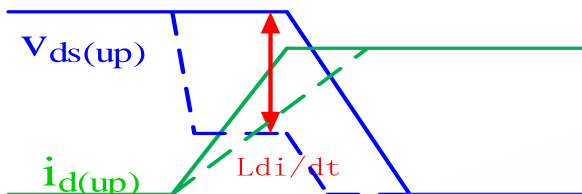
Fig. 5: switching node waveforms of eGaN FET and MOSFET designs (V_{IN}=48 V, I_{OUT}=10 A, f_{sw}=300 kHz, Gen 4 GaN transistors: EPC2021, Gen 2 GaN transistors: EPC2001, MOSFETs: BSZ123N08NS3G)

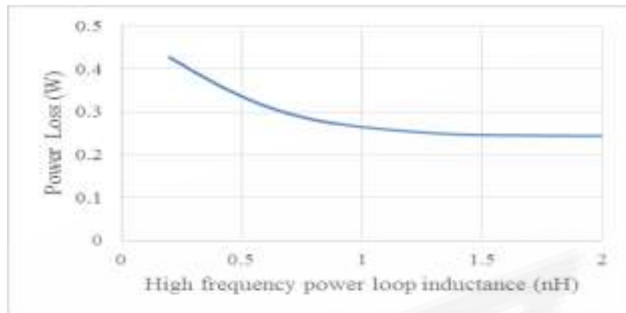
Alex Lidow and David Reusch Efficient Power Conversion Corporation. A New Generation of Power Semiconductor Packaging Paves the Way for Higher Efficiency Power Conversion

漏源回路寄生电感问题

- 漏源回路寄生电感导致额外的开关损耗

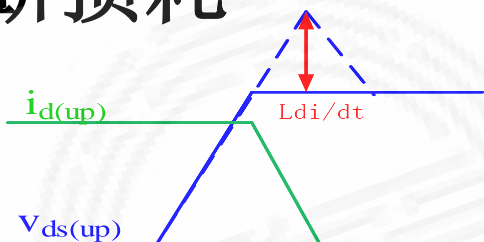
开通损耗

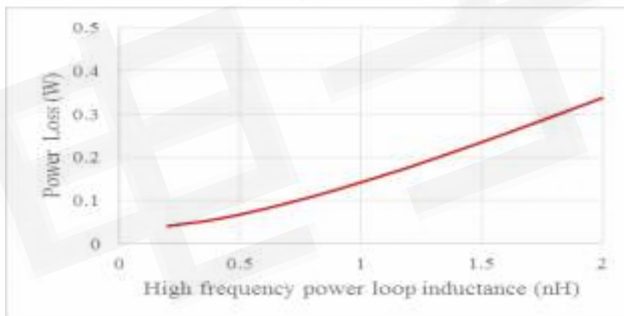




- L_D 对开通过程的影响
  - 减小了电压电流交叠损耗
  - 使寄生振荡加剧、损耗增加
  - 总体来看，L_D增大开通损耗呈减小的趋势

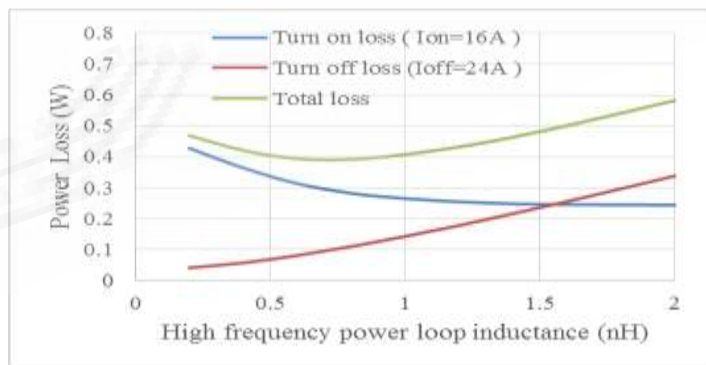
关断损耗





- L_D 对关断过程的影响
  - 增大了交叠面积、损耗增加
  - 使寄生振荡加剧、损耗增加
  - 总体来看，L_D增大关断损耗呈上升的趋势

总开关损耗



- ZVS 工作

  L_D越小，开关损耗越小

- 硬开关工作

  存在最优的L_D，使开关损耗最小

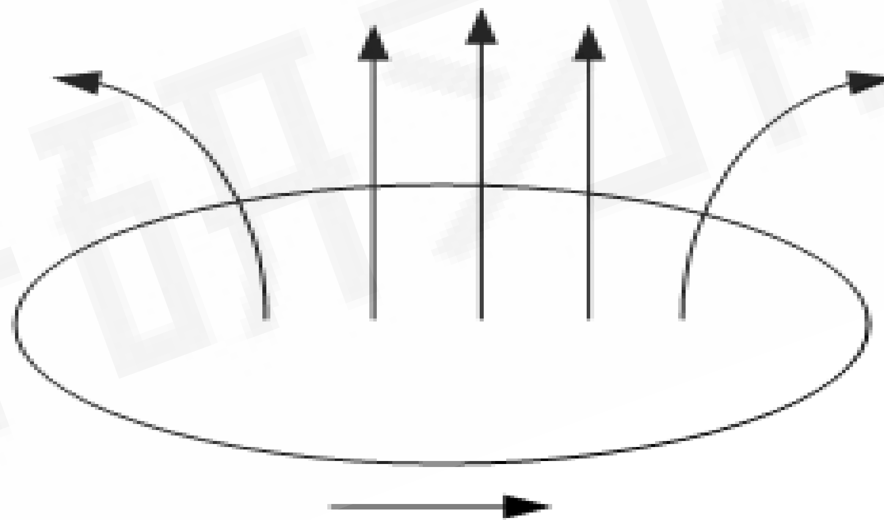
漏源回路寄生电感问题

- 影响回路电感的因素

$$L = \frac{\psi}{I}$$

$$\psi = N\iint_S B ds$$

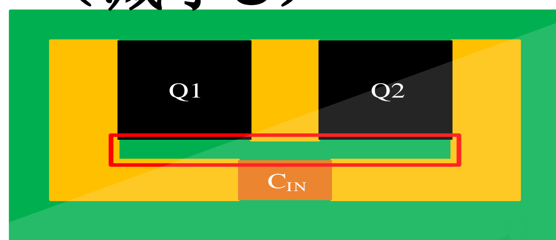
匝数　　回路面积　　磁感应强度



漏源回路寄生电感问题

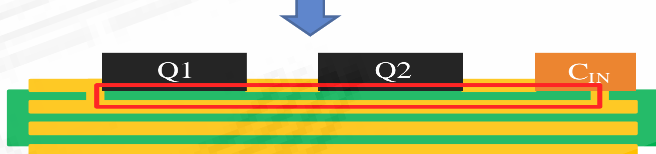
- 降低功率回路的寄生电感的方法

1. 减小功率回路面积（减小S）



Horizontal loop

Vertical loop I



Vertical loop II

2. 增加屏蔽层，利去磁效应（减小B）

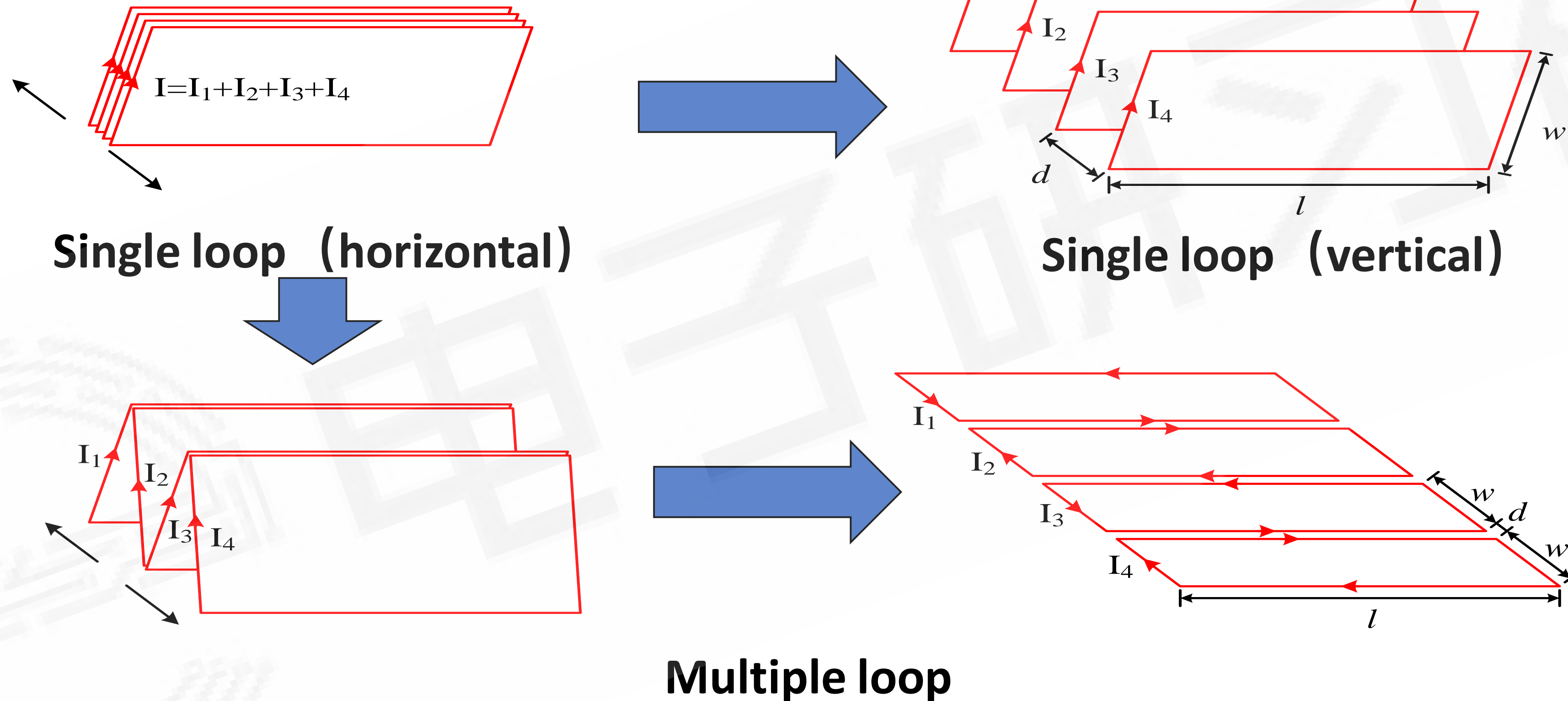
Horizontal loop with shielding layer

*D. Reusch, and J. Strydom, “Understanding the Effect of PCB Layout on Circuit Performance in a High-Frequency Gallium-Nitride-Based Point of Load Converter,” *Power Electronics, IEEE Transactions on,* vol. 29, no. 4, pp. 2008-2015, 2014.

**Y. Xi, M. Chen, K. Nielson, and R. Bell, "Optimization of the drive circuit for enhancement mode power GaN FETs in DC-DC converters," in Applied Power Electronics Conference and Exposition (APEC), 2012, pp. 2467-2471.

漏源回路寄生电感问题

3. 多回路并联（降低耦合）

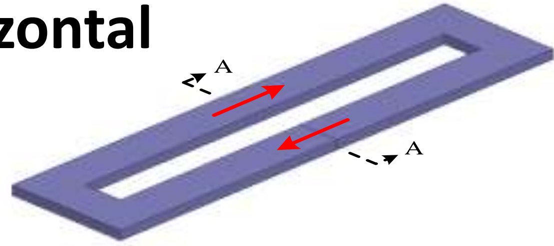


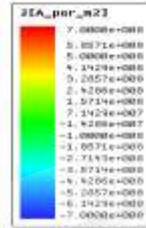
- Loop inductance is reduced when total flux is reduced.

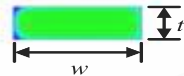
$$L = \frac{\psi}{I}$$

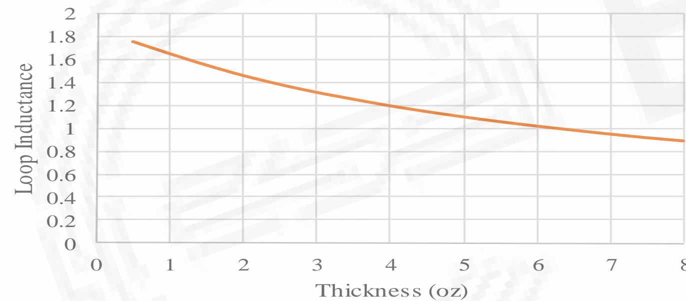
漏源回路寄生电感问题

horizontal



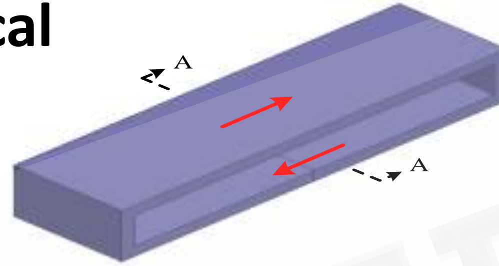


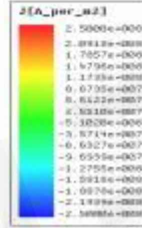


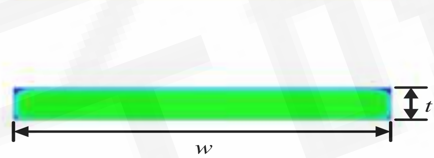


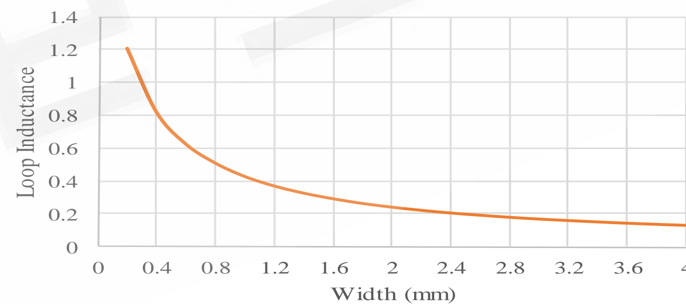
厚度

vertical



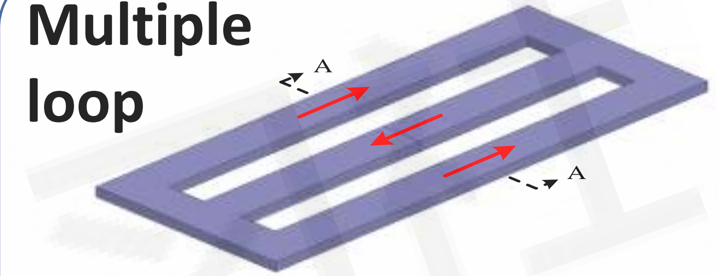


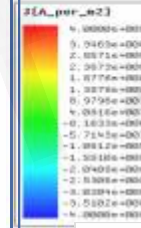


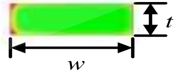


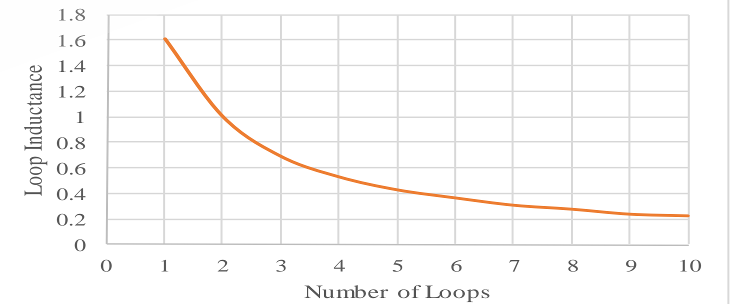
宽度

Multiple loop









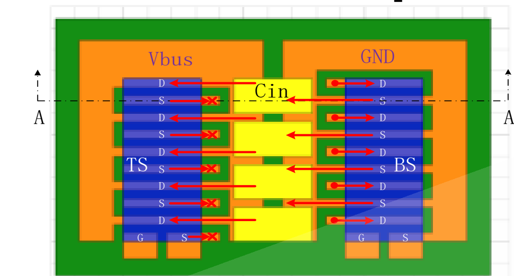
回路数

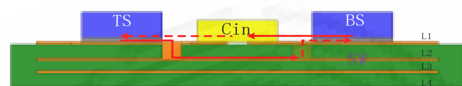
- **To reduce loop inductance:**
  - **wider trace**
  - **Multiple loop： more loops**

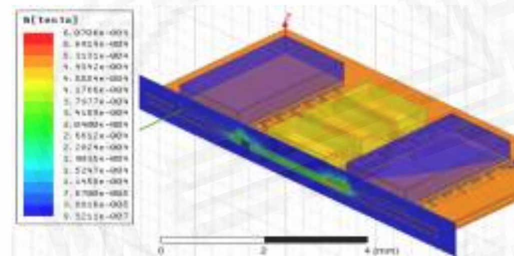
漏源回路寄生电感问题

- 实现方案

Parallel loop 1

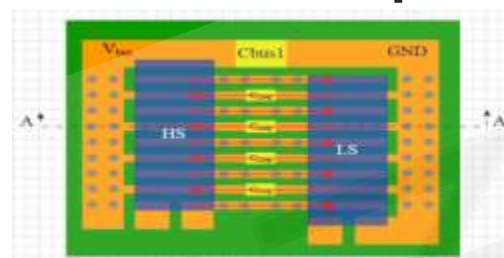


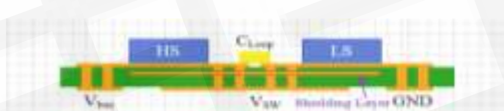


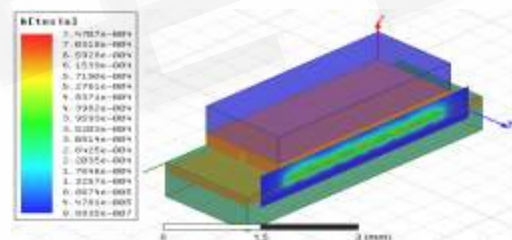


0.22nH

Parallel loop 2

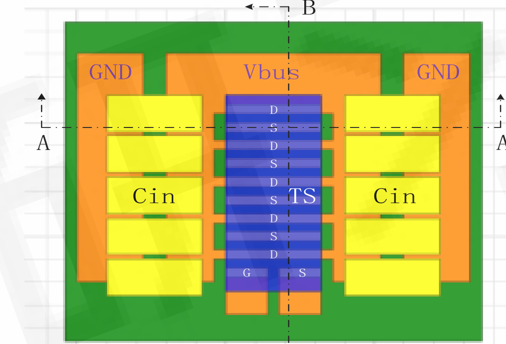


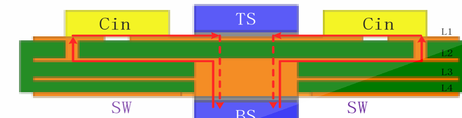


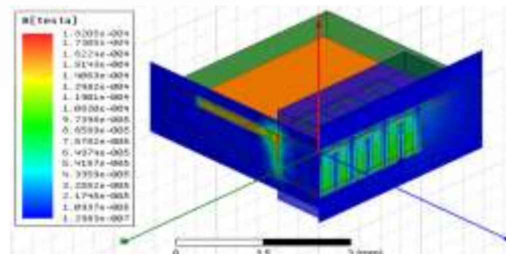


0.2nH

Double side

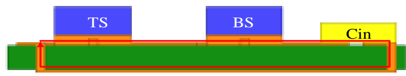


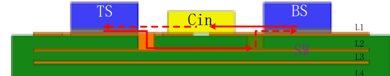


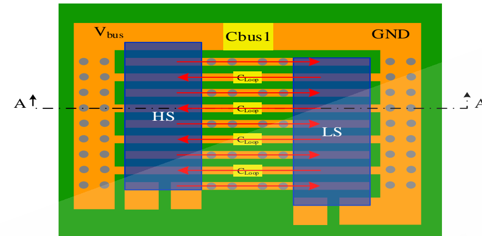


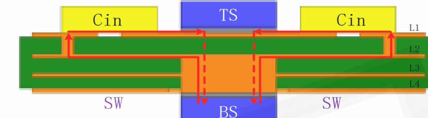
0.1nH

漏源回路寄生电感问题







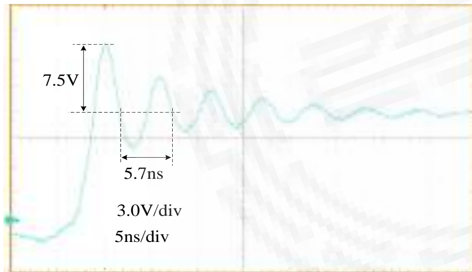


Bench mark
15mm*15mm

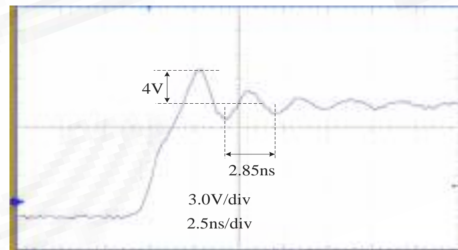
Parallel loop 1(**0.22nH**)
15mm*15mm

Parallel loop 2 (**0.2nH**)
9mm*9mm

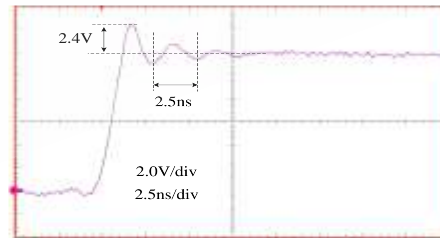
Double side(**0.1nH**)
15mm*15mm



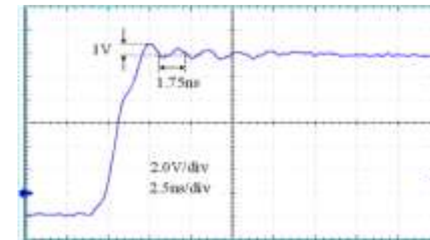
Bench mark
(**0.9nH**)



Parallel loop 1
(**0.22nH**)

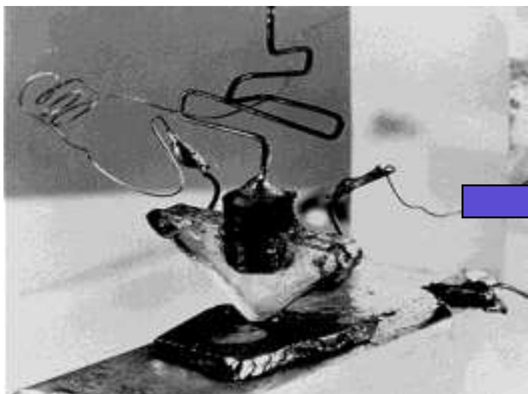


Parallel loop 2
(**0.2nH**)



Double side
(**0.1nH**)

集成化——集成电路的故事

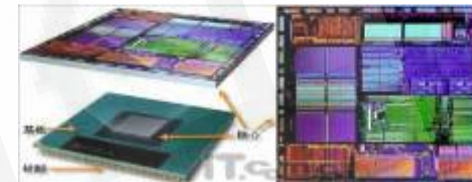


First Transistor invented in 1947

Jack Kilby's first working integrated circuit, tested on September 12, 1958,

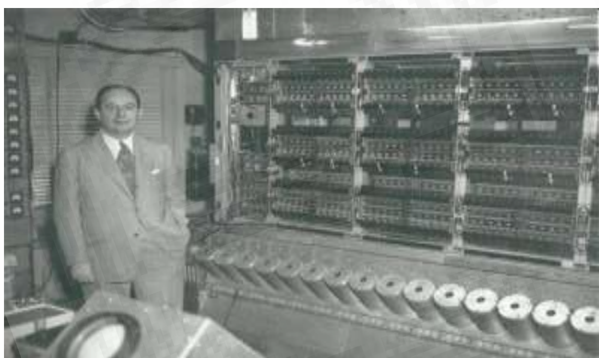
Small scale IC

No. of ***Transistors<100***



Modern CPU

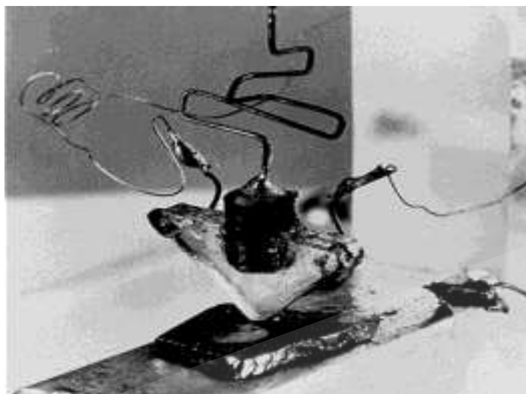
No. transistors ~1billium



ENIAC & von neumann

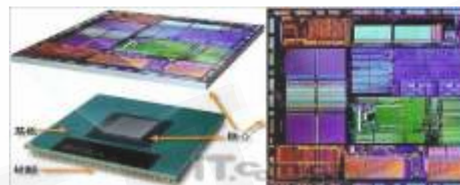
iphone & Steve Jobs

电力电子集成没有那么简单



First Transistor invented in 1947

体积缩小10亿倍



Modern CPU
No. transistors ～1billium

体积缩小1000倍

IBM PC/XT power supply 1983： 63.5W

Power density: ~1W/in3

Efficiency: ~60％

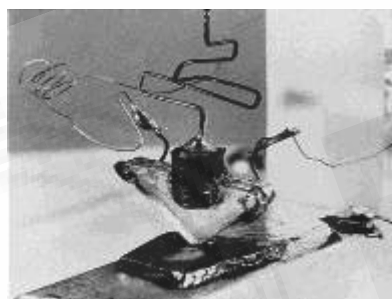
VTM from Vicor : 100A/300W

Power density: ~1000W/in3

Efficiency:97~99%

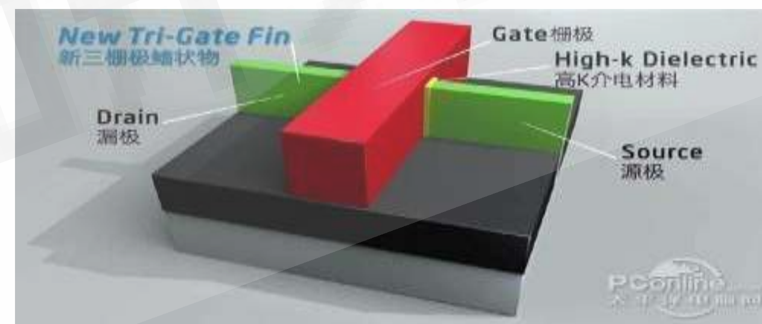
电子电路高度集成化的原因

- 数字电路的逻辑功能不随元件缩小而变化
- 仅数字电路能够通过大规模集成化来缩小体积



Voltage:~10V
Current:~0.1A
Logic gate:1

Shrink size
for 1B times

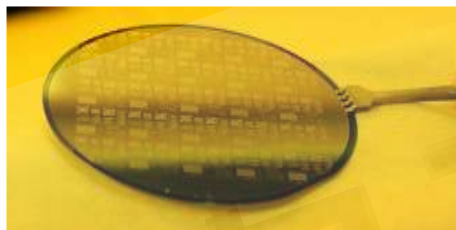


Voltage:~10V
Current:~1nA
Logic gate: 1

电力电子集成的难点

- 电力电子元件(含模拟电路元件)的尺寸取决于电流或储能，受材料物理极限的制约 (λ, μ, ε).

半导体



→ 芯片面积正比于电流

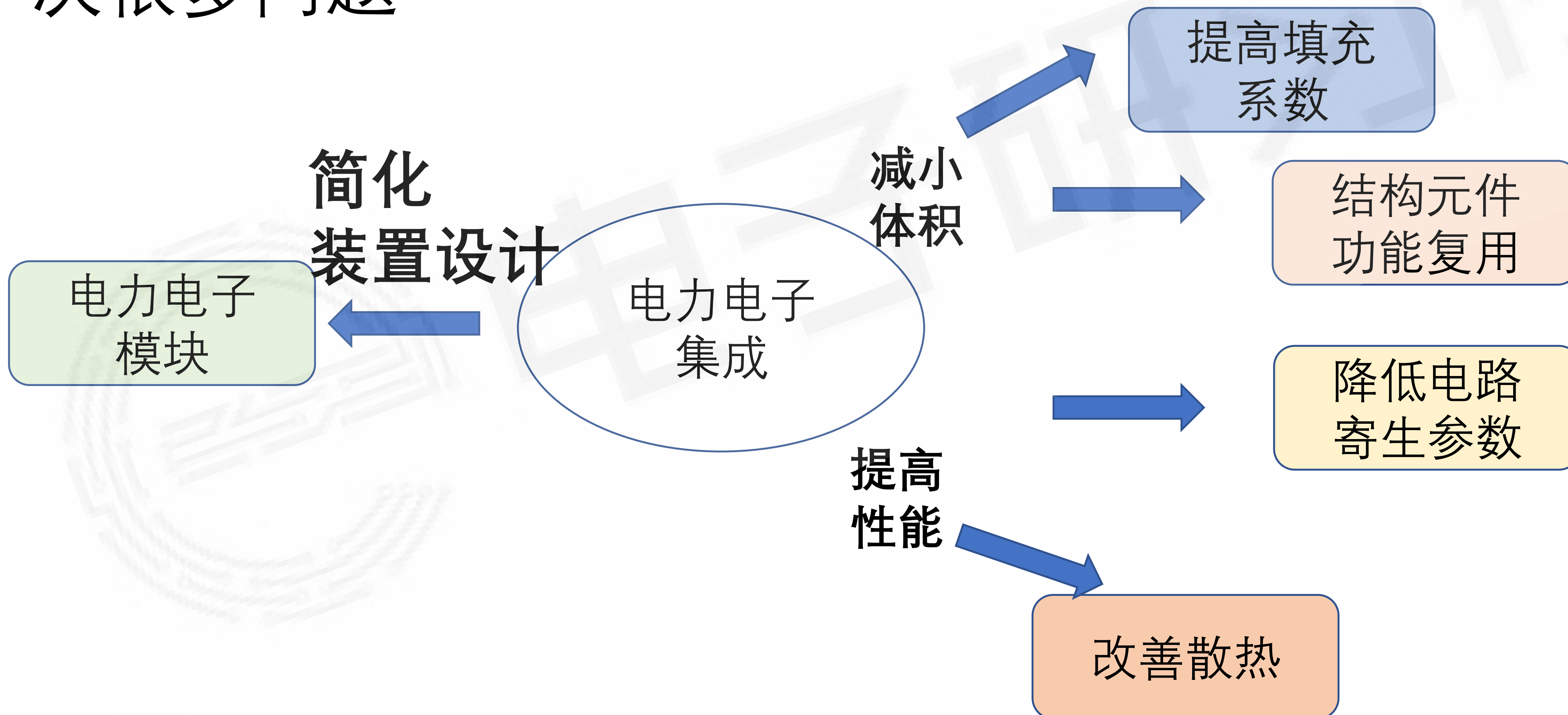
电感电容元件

→ 元件体积正比于储能

电子研习社

电力电子集成的目标

- 虽然不能大幅度缩小体积，电力电子集成还是可以解决很多问题



电力电子集成方案(半导体部分)

单片集成(低功率)

Monolithic Integration

Integrated inductor

混合集成(高功率)

Active Switch

裸芯片

MCM

Interconnection Process

WireBond

Solder Bump
Dimple on Copper Flex
Underfill
Al Pad
Silicon Chip
UBMPassivation

Double Side Soldering

Dielectric
Components
Metallization
Solder
Ceramic
Substrate

Thin Film

驱动芯片
固定螺钉
PCB板
发射极板
压接簧片
铜过渡片
IGBT管芯
DBC板
铜基板
栅极键合铝丝
互连引线

Pressure Contact

Power Module

DrMOS

IPM:IGBT+Driver

Semikron

Skiip:IGBT+Driver +HeaSink

IPEM: IGBT+Driver+Control (Integrated)

Infineon

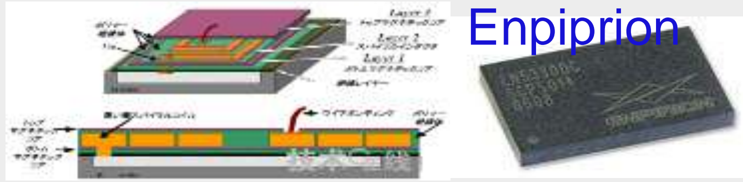
Stack:IGBT+Driver+ HeatSink+Bus+Cap

American Super conductor

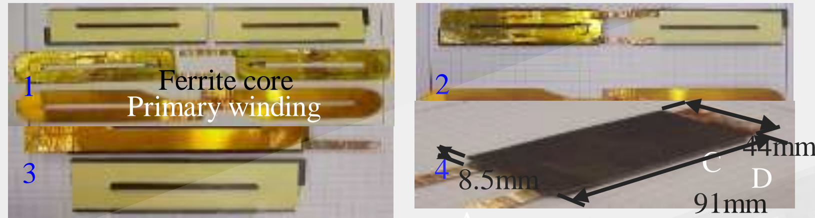
PEBB:IGBT+Driver+ HeatSink+Bus+Cap +Control+Comm.

无源元件的集成化

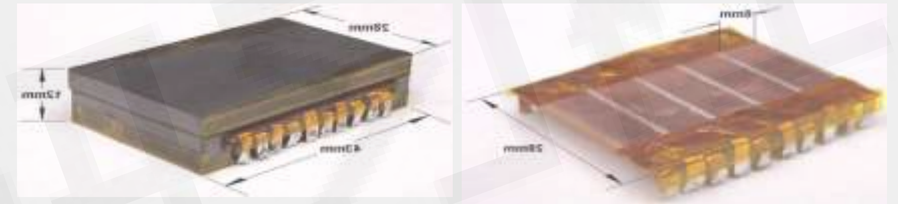
Thin film



Assembly

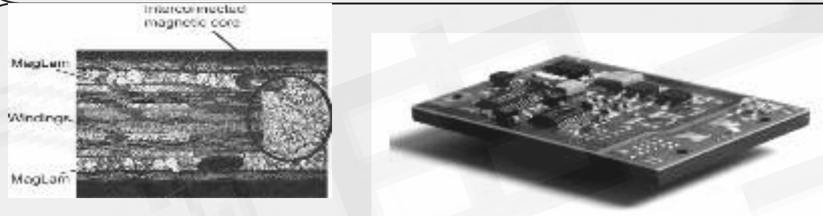


Planar LCT CPES

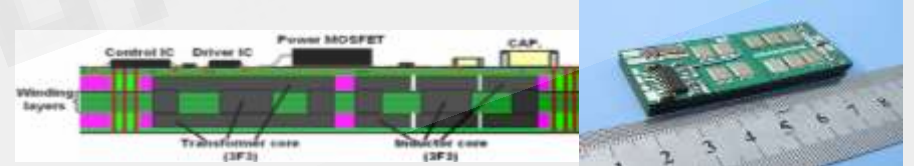


Planar LCT CPES

Laminate



MagLam TU Delf/Phillips



Embedded Ferrite
XJTU Perec/CPES/TU Delft

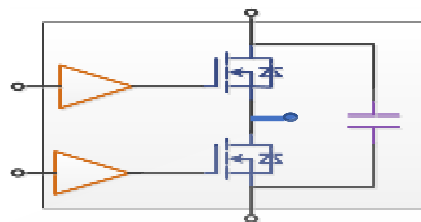
Co-Firing

LTCC CPES/ XJTU PEREC

Thick film

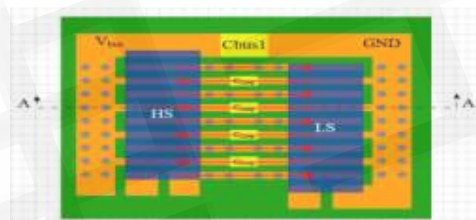
GaN器件的集成化

电路优化



Solution 4:
With Bus
cap./driver

布线优化



Parallel loop 2

散热优化

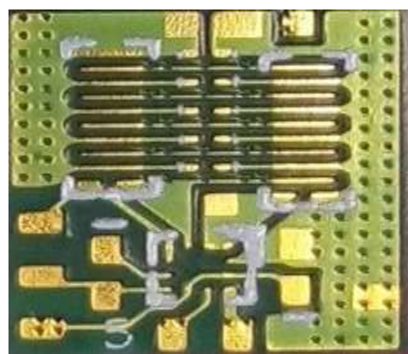
- AlN substrate
- Substrate size： 9*10mm
- Device distance: 4mm

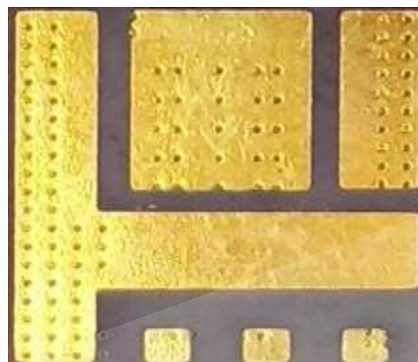
GaN 器件
AlN
DBC
过孔
焊盘

GaN器件集成模块

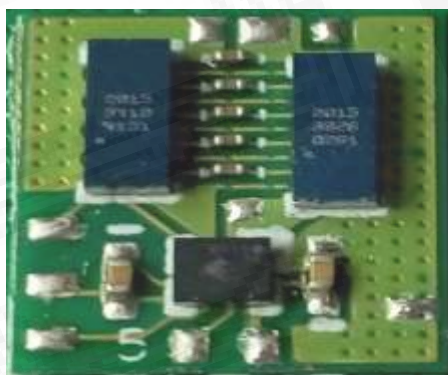
*受台达环境与教育发展基金项目资助

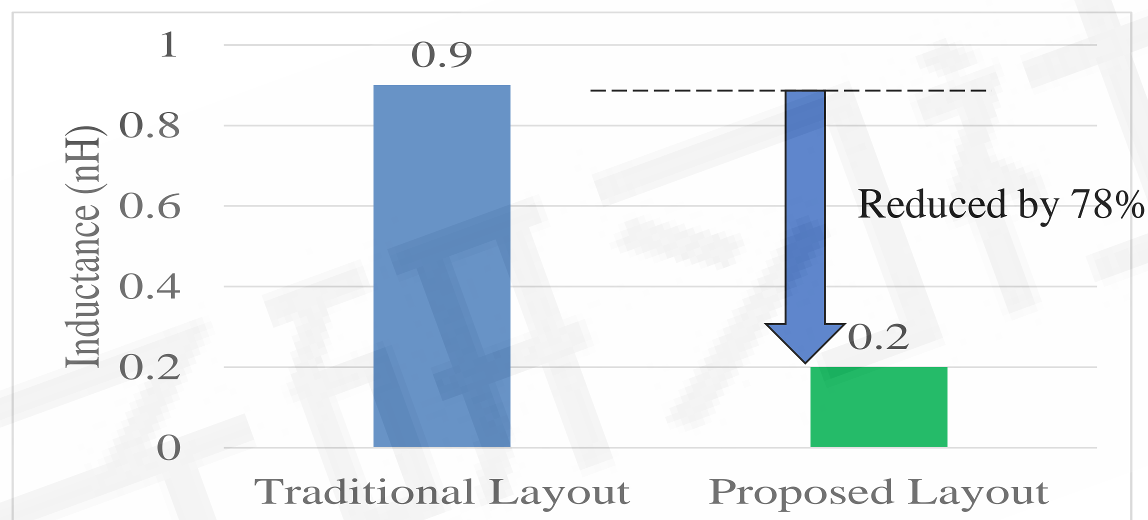
GaN集成模块的低电感布线

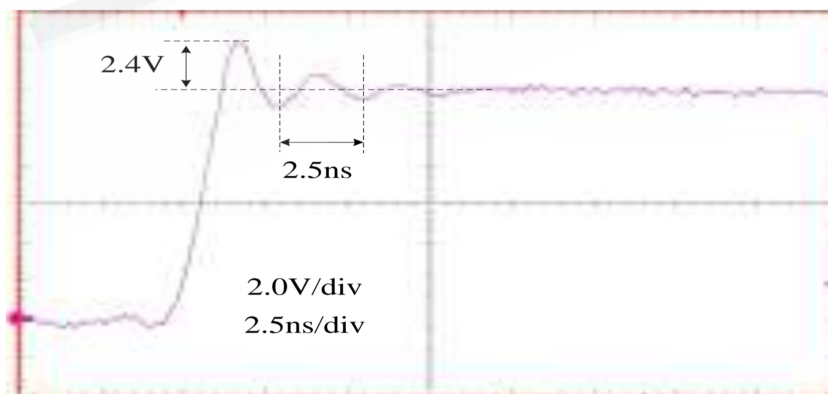

Topside


Bottom side

AIN substate（9mm*10mm）


Integrated module

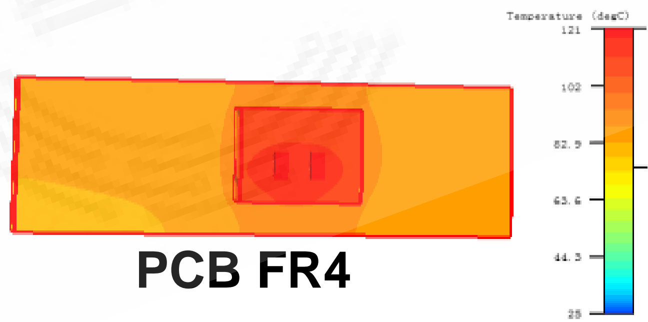




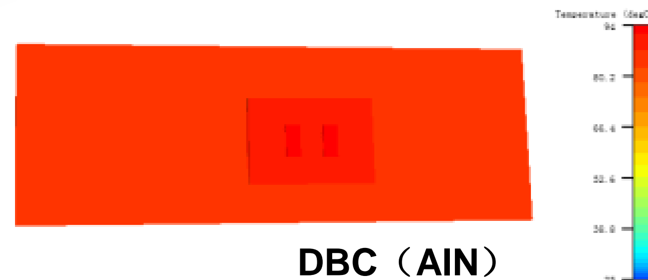
集成模块基板材料的选择

- 采用高热导率材料基板安装GaN器件，可以改善散热

材料	PCB(FR4)	DBC(Al_2O_3)	DBC(AlN)	LTCC	Diamond
热导率 Thermal conductivity ($Wm^{-1}K^{-1}$)	0.3	25	180	3.3	2000
热阻Rth natural cooling （K/W）	46	37	31.85	40.5	24.75
热阻Rth forced convection （K/W） (flow speed 5m/s)	27.25	14.6	13.75	17.8	10.85



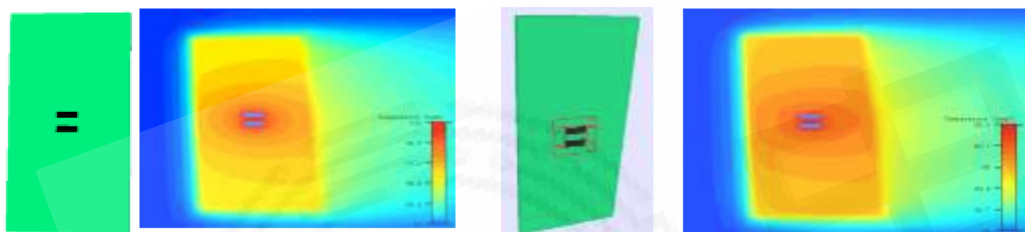
PCB FR4

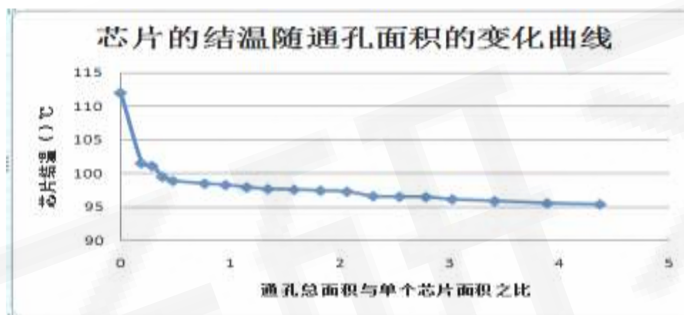

DBC（AIN）

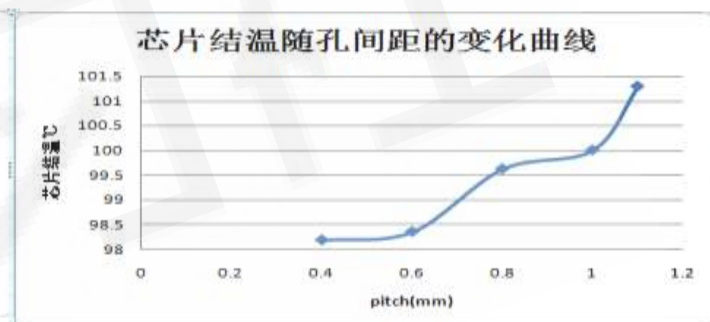
导热通孔的效果

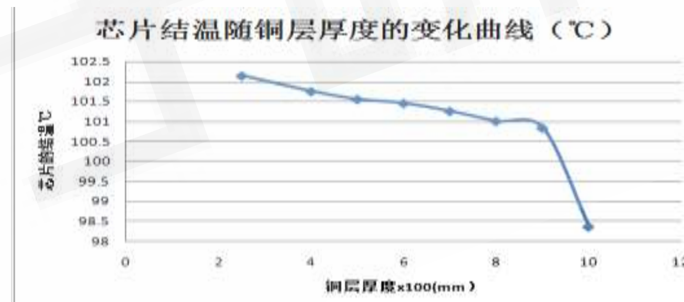
- 在PCB基板中布置导热通孔，也能改善散热

未添加热通孔　　添加导热通孔









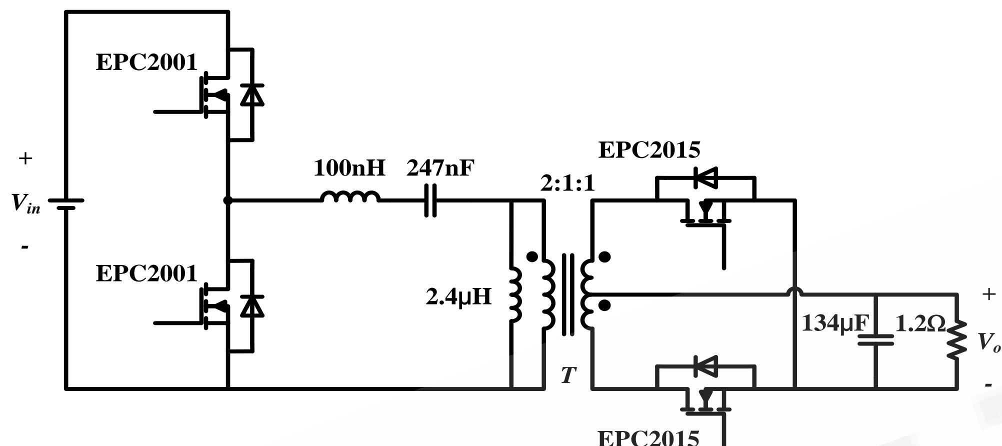
*GaN器件各设置为1W损耗，通孔尺寸：直径0.2，壁厚0.1，间距0.6

	无导热通孔	有导热通孔
$Rth_{J\text{-}A}$ (K/W)	43.4	36.65

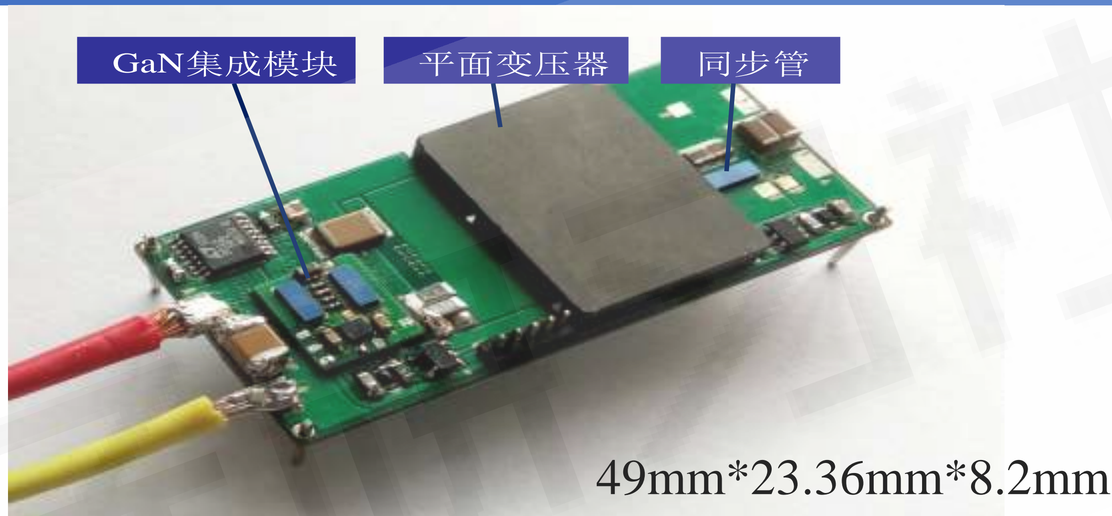
导热通孔设计导则：

- 通孔覆盖面积要与器件尺寸相比拟。
- 工艺允许的情况下尽量减小孔间距。
- 工艺允许时应尽量完全填充。

GaN集成实例1：LLC 变换器

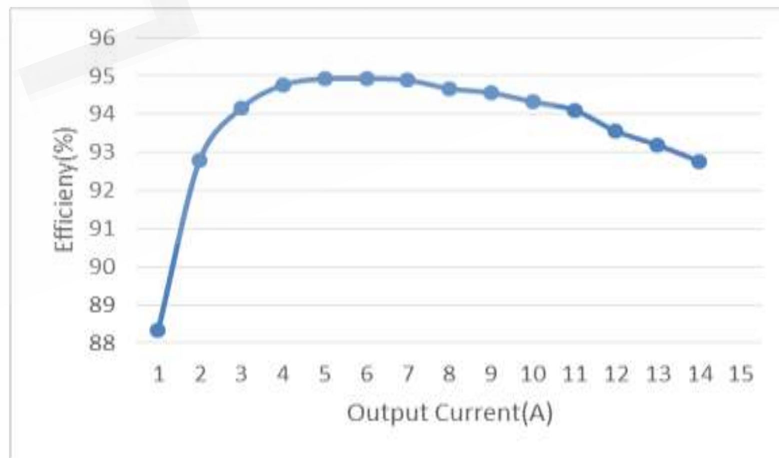


LLC 变换器



LLC 变换器原型

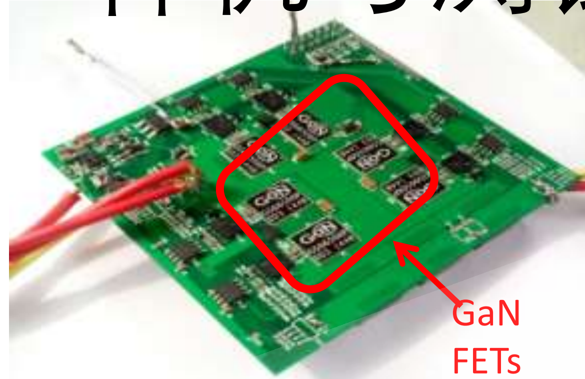
输入电压	48V
输出电压	12V
输出功率	200W
开关频率	1MHz
所用器件	EPC2001 (100V, 25A)



效率

GaN集成实例2： 2kW高密度单相逆变器

- 样机与测试结果

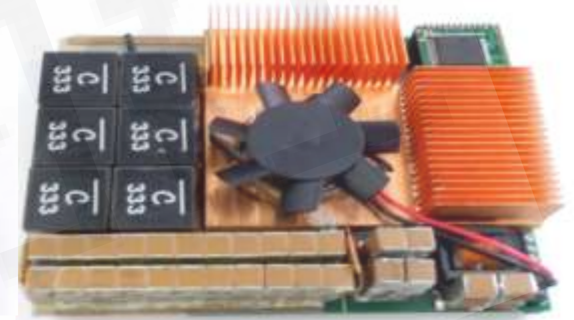


7.8cmX8cmX1.3cm
正面

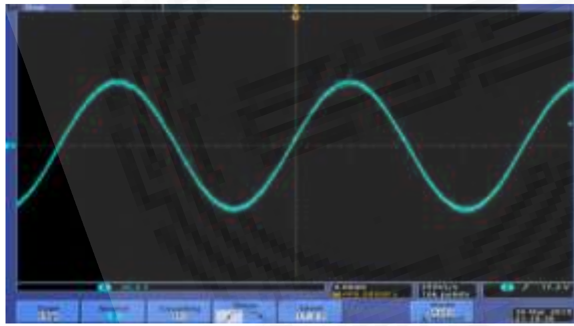
反面

PCB基板结构方案

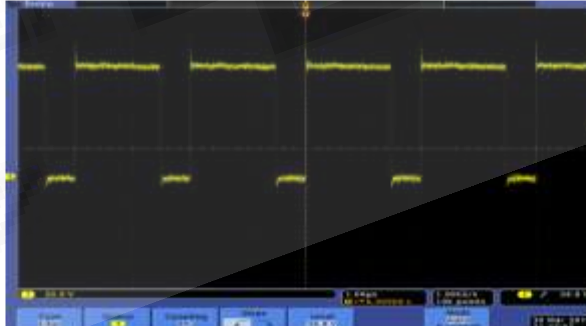
正面



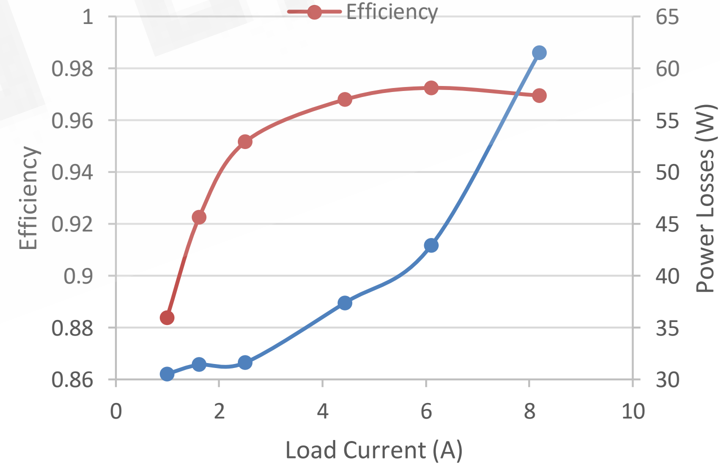
反面



输出电压波形



桥臂中点电压波形



效率和损耗曲线

小结

GaN器件与硅器件的对比

- ✓ 低通态电阻（ Rdson ）、低通态损耗,
- ✓ 低驱动电荷、高开关速度、低开关损耗.
- × 对寄生电感参数敏感、驱动难度大、面积太小散热差.

GAN器件应用导则

- ✓ 高频应用时开通损耗还比较显著,应采用 ZVS 开关方式.
- ✓ 必须优化布线减小功率回路的寄生电感，否则难以控制开关过程产生的寄生振荡和过电压。.
- ✓ 需要提高基板的散热能力来改善散热，常见方法是采用高热导率基板和增加热过孔.

通过集成化可以很好的解决GaN器件应用的难点问题，是GaN器件应用的关键技术.

Q&A？

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